Name: **Enrolment No:**	UPES UNIVERSITY OF TOMORROW

UPES
End Semester Examination, May 2025

Course: **Semester:**
Program: **Time : 03 hrs.**
Course Code: **Max. Marks: 100**

Instructions:

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Perform the following conversions a) Convert 50 to binary representation b) Convert $(101011)_2$ to decimal c) 0xFFE to decimal d) 34 to -34 using 2's complement		**CO1**
Q2	What is addressing mode and list different types of addressing modes		**CO4**
Q3	What is a hardwired control unit, its working principle and the different advantages and disadvantages		**CO3**
Q4	Showcase your understanding of the memory hierarchy using the memory hierarchy diagram		**CO4**
Q5	An I/O interface has the following status register format: • Bit 0 represents if the device is ready or not (1 means it is ready) • Bit 1 represents if there is any error (1 means there is an error) • Bit 2 represents the flow of data direction (1 means it is in input mode) • Bits 3 to 7 are reserved Interpret the status register value 0x02		**CO3, CO4**

SECTION B
(4Qx10M= 40 Marks)

Q6	Discuss about the Flynn's taxonomy with a diagram and identify the following systems according to the Flynn's taxonomy with proper reasoning A traditional single core CPU • A GPU processing an Image • A cluster of computers solving different parts of the same problem • A fault-tolerant system with redundant proessing		**CO4**

<table>
<tr><td>Q7</td><td>Discuss the three types of data transfer methods the CPU communicates with I/O devices</td><td></td><td>CO4</td></tr>
<tr><td>Q8</td><td>List down the stages in a four-stage pipeline and explain using the pipeline diagram</td><td></td><td>CO5</td></tr>
<tr><td>Q9</td><td>Explain the RISC and CISC architectures and draw comparison between them in a tabular format
(Or)
Explain about three address, two address, one address and zero address instruction formats and provide the code for each using the example problem (A + B) * (C – D)</td><td></td><td>CO2, CO3</td></tr>
<tr><td colspan="4">SECTION-C
(2Qx20M=40 Marks)</td></tr>
<tr><td>Q9</td><td>Discuss the different types of cache memory principles along with their respective diagrams
(Or)
Discuss about Hardwired Control Unit, Microprogrammed Control Unit and their working principles. Finally, draw a comparison between these two.</td><td></td><td>CO1, CO4, CO5</td></tr>
<tr><td>Q10</td><td>Solve all of the following problems
• A System with three interrupt sources has the following characteristics
<table>
<tr><th>Device</th><th>Priority</th><th>ISR Time</th><th>Frequency</th></tr>
<tr><td>Disk</td><td>High</td><td>50 μs</td><td>100/sec</td></tr>
<tr><td>Network</td><td>Medium</td><td>30 μs</td><td>200 /sec</td></tr>
<tr><td>Keyboard</td><td>Low</td><td>10 μs</td><td>500 /sec</td></tr>
</table>
Calculate the percentage of CPU time spent handling interrupts

• Analyze the following code for pipeline hazards and propose solutions and ensure to include an optimized pipeline diagram:
LOAD R1 , A // Load A i n t o R1
ADD R2 , R1 , 5 // Add 5 to R1 , s t o r e i n R2
MUL R3 , R2 , R2 // Square R2 , s t o r e i n R3
BRZ R3 , Label // Branch i f R3 i s zero

Assumptions are:
• 5-stage RISC pipeline (IF, ID, EX, MEM, WB)
• No forwarding/bypassing initially
• Separate memory access unit</td><td></td><td>CO4, CO5</td></tr>
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