Name: **Enrolment No:**	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2021

Programme Name: B. Tech (Electronics & Communication Engineering) **Semester : VII**
Course Name : VLSI Design **Time : 3:00 hrs**
Course Code : ECEG-4001 **Max. Marks: 100**
Nos. of page(s) : 02
Instructions: Assume any data in programming, if required.

SECTION A (4 x 5 = 20 Marks)

Attempt *all* the questions

Q.1 Explain the significance of body effect in MOSFET. [4] [CO1]

Q.2 Detail the followings with respect to MOSFET circuits. [4] [CO4]
(a) Zipper CMOS
(b) Power delay product
(c) Propagation delay
(d) Noise Margin

Q.3 Write the all steps in the FPGA Design or ASIC Design flow. [4] [CO5]

Q.4 What is the need of low power CMOS circuit design? Draw the voltage transfer characteristics of NMOS. [4] [CO4]

Q.5 Detail the logic simulation of synchronous positive edge D Flip-flop using VHDL. [4] [CO5]

Section-B (4 x 10 = 40 Marks)

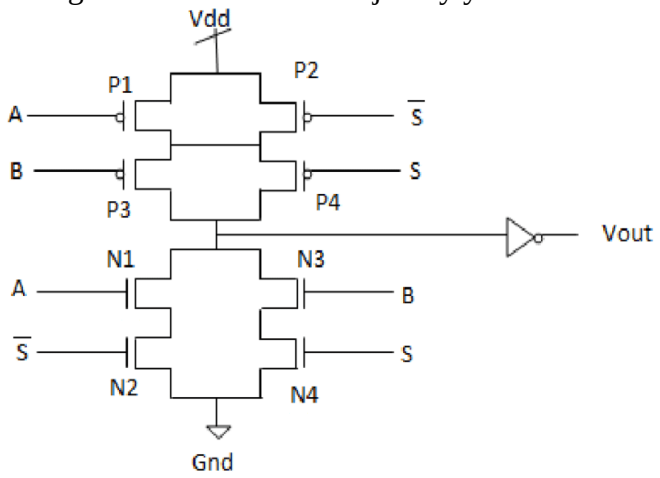
Attempt *all* the questions

Q.6 Detail the functionality of enhancement type NMOS under different regions. Derive the mathematical equations of the drain current for NMOS in all the regions. [10] [CO1]

Q.7 (a) Realize the following functions using NMOS and CMOS. [6]

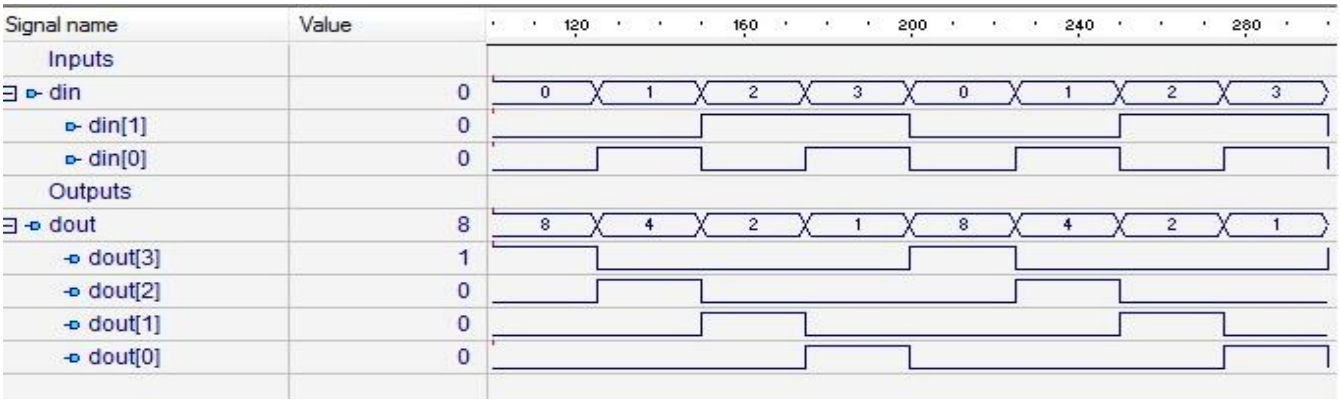
$$Y = \overline{A.(B + CD)}$$
$$Y = \bar{A}\bar{B} + \bar{C}$$

(b) Write the output of the logic diagram shown below and justify your answer. [4] [CO4]



Q.8 Write the detailed steps in CMOS fabrication using Twin Tub process. [10] [CO2]

Q.9 (a) Draw the logic diagram to support the following timing waveform and develop the code in VHDL to support the functionality. [10] [CO5]



OR

(b) What are the different styles of modeling in VHDL? Design (8 x 1) multiplexer using any two styles of modeling, logic diagram and timing simulation waveform.

Section-C (2 x 20 = 40 Marks)

Attempt the followings

Q.10 (a) Draw the parasitic capacitance model of MOSFET.

Consider a process technology for which L_{min} = 0.4 μm, tox = 8 nm, μ_n = 450 cm^2/ V-s and V_t = 0.7 V

(i) Find C_{ox} and K'_n

(ii) For a MOSFET with W/ L = 8 μm/0.8 μm, Calculate the value of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_D =100μA.

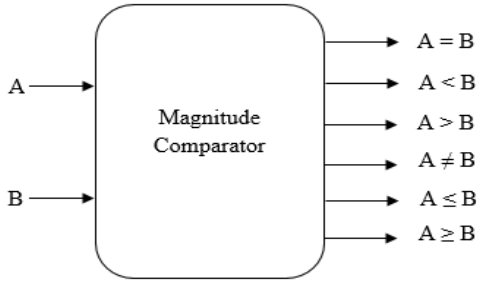
(iii) For the same device, find the value of V_{GS} required to cause the device to operate as a 1000 Ω resistor for very small V_{DS}. [20] [CO3]

OR

Q.11 (a) Draw the voltage transfer curve for the CMOS inverter and derive the mathematical expression to estimate the value of V_{OH}, and V_{IL} for CMOS inverter circuit and detail the functionality. [10] [CO3]

(b) Draw the CMOS logic layout and stick diagram of inverter, 2 input NAND and NOR gates. [10] [CO3]

Q.12 The purpose of a digital comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …. An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison. For example, a magnitude comparator of two 1-bits, (A and B) inputs would produce the following three output conditions when compared to each other. This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the case of 64-bit comparator for the different logic functions.



(a) Develop the VHDL/ Verilog HDL code to support the functionality of design

(b) Estimate the different test cases and test benches of the design.

(c) Design an ALU chip that accepts 32-bit data and perform at least 10 operations using VHDL. [20] [CO5]