Study of Memristor and Development of Applications Based on Memristor

A thesis submitted to the
University of Petroleum & Energy Studies

For the Award of
Doctor of Philosophy
in
Electronics Engineering

By
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September, 2020

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Declaration

I declare that the thesis entitled **“Study of Memristor and Development of Applications Based on Memristor”** has been prepared by me under the guidance of Dr. Adesh Kumar, Internal Supervisor, Associate Professor, School of Engineering, Department of Electrical & Electronics Engineering, University of Petroleum & Energy Studies, Dehradun and Dr. Anurag Srivastava, Professor, Department of Information Technology, Atal Bihari Vajpayee Indian Institute of Information Technology, Gwalior. No part of this thesis has formed the basis for the award of any degree or fellowship previously.

Manish H. Bilgaye
Dated: 25/09/2020

CERTIFICATE

This is to certify that the thesis entitled **"Study of Memristor and Development of Applications Based on Memristor"** is being submitted by **Mr. Manish H. Bilgaye** in fulfillment for the Award of DOCTOR OF PHILOSOPHY in (Electronics Engineering) to the University of Petroleum and Energy Studies. Thesis has been corrected as per the evaluation reports dated 25/09/2020 and all the necessary changes / modifications have been inserted/incorporated in the thesis.

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ABSTRACT

Developments in electronics engineering coupled with computer science engineering have shown us an aspect of the world we visualize currently. Another aspect is natural and constant evolution process which by all means is not going to stop. With current interdisciplinary technological developments we see scientists staying in space stations, on the verge of volcanoes, deep seas and forests, in laboratories and in open for elongated time durations performing experiments on range of disciplines thereby reaching the edge of the innovations thereby challenging current technology for furtherance to new unknown realms. In the process, they unravel the hurdles successfully and keep on asking for answers for solutions. One source is common for all and it is computation and if computation changes the way it is now then it will be information technology computation explosion.

Associated people are asking for solutions like computation and processing of the data while traveling on the data bus and prior to reaching to the CPU/architecture of the microprocessor. Second demand is memories with enhanced storage capacity while consuming little or no power. Third aspect is multilevel storage capability per bit of memory leading to non-binary computations followed by developments in the areas like robotics, artificial intelligence, data mining, etc.

However, a new fourth fundamental passive component Memristor is capable to address all these demands and possesses the capacity to revolutionize the electronics and computation sciences. However, it needs intense research and integration of many disciplines to fructify as a technology and the entire scientific community is joining hands to make it a reality.

This thesis explores range of materials for memristive behavior, classifies the physical phenomenon responsible, fits it into the characteristics *V-I* fingerprint

defined, and explore its application as nonvolatile memory. The methodology includes identification of the physical parameters responsible, fit their behavior mathematically and simulate analog behavior using the SPICE environment and digital aspect using Modelsim and Xilinx environment. The results have been shown as transient analysis of phase change cell and variability with temperature has been explored.

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For my parents, I have no words but just feelings. I owe my being to them.

DEDICATION

To Almighty

My Wife Mrs. Kalpana and Children Master Shashank and Master Atharva

Respected Uncleji and Auntieji Dr. T. C. Pokhriyal and Mrs. Prabha Pokhriyal

Respected Uncle M. L. Mittal

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Acronyms

ReRAM	Resistive Random Access Memory
RRAM	Resistive Random Access Memory
MEMory ResISTOR	MEMRISTOR
Ge	Germanium
Se	Selenium
Sb	Antimony
In	Indium
Pt	Platinum
TiO_2	Titanium dioxide
TiO_{2-x}	Titanium dioxide deficient of oxygen
M(q)	Memristance
Ni	Nickle
Ti	Titanium
Nb	Noibium
Zr	Zirconium
Cu	Copper
Ag	Silver
Cu(S)	Copper Sulphide
RS	Reset/Set mechanism
ZrO_2	Zirconium dioxide
Ta_2O_5	Tantalum pentoxide
SiO_X	Silicone oxide

Al_2O_3	Aluminium oxide
PCM	Phase Change Memory
PCMC	Phase Change Material Memory Cell
M-I	Metal-Insulator
Au	Gold
SiO	Silicon monoxide
VO2	Vanadium oxide
As	Arsenic
Te	Tellurium
I	Iodine
PCRAM	Phase Change Random Access Memory
PRAM	Phase Change Random Access Memory
CRAM	Chalcogenide Random Access Memory
3D	Three dimension
IBM	International Business Machine
ERD	Emerging Research Devices
NRI	Nanoelectronic Research Initiative
AI	Artificial Intelligence
HP	Hewlett Packard
CAD	Computer Aided Drafting/Designing
GPU	General Processing Unit
CD	Compact Disk
DVD	Digital Versatile Disk
HD	High Definition Blue Ray Disk

HDD	Hard Disk Drive
CuO	Copper oxide/Cupric oxide
NiO	Nickel oxide
CoO	Cobalt oxide
Fe_2O_3	Ferric oxide
MoO	Molybdenum oxide
Cu_2S	Copper sulphide
Ag_2S	Silver sulphide
Si	Silicon
GaAs	Gallium Arsenide
ZnSe	Zinc Selenide
$SrTiO_3$	Strontium titanate
Cr	Chromium
CA_XMnO_3	Calcium titanium oxide
CuPc	Hyperbranched copper phthalocyanine
H	Hydrogen
SAM	Self Assembled Monolayer
PEDOT:SS	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
GO	Graphene oxide
PZT	Zirconate titanate
MIM	Metal Insulator Metal
NDR	Negative Differential Resistor
ISE	Integrated System Environment
MLC	Multi Level Cell

RESET	High Resistance State of Resistive Random Access Memory Cell
SET	Low Resistance Sate of Resistive Random Access Memory Cell
SPICE	Simulation Program with Integrated Circuit Emphasis
ITRS	International Technology Roadmap for Semiconductors
FET	Field Effect Transistor
RTL	Register Transfer Level
LCD	Liquid Crystal Display
i-DAC	Current Digital to Analog Converter
LUT	Look Up Table
IoB	Input Output Block
GLCK	Gated Clock
MHz	Mega Hertz
ROM	Read Only Memory
EDK	Embedded Development Kit
ZBT	Zero Bus Turnaround
PHY	Physical Layer
GMII	Gigabit Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
SGMII	Serial Gigabit Media Independent Interface
USB	Universal Serial Bus
SAC	Stereo Audio Codec
SPDIF	Sony/Philips Digital Interface Format

I/O	Input/Output
RS232	Recommended Standard Number 232
CGROM	Character Generator Random Read Only Memory
CGRAM	Character Generator Random Access Memory
DDRAM	Display Data Random Access Memory
IR	Instruction Register
RS	Register Strobe
R/W	Read/Write
UCF	User Constraint File
HDL	Hardware Description Language

List of Abbreviations

R	Resistor
C	Capacitor
L	Inductor
M	Memristor
v	Voltage
i	Current
q	Charge
φ	Flux
τ	Time period
w	Width (Dimension of Memristance)
V-I	Voltage-Current Characteristics
w/D	Normalized state variable
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
FLASH	A type of memory
FPGA	Field Programmable Gate Array
EDA	Electronic Design Automation
CMOS	Complementary metal oxide semiconductor
MOS	Metal oxide semiconductor
K	Kelvin
A/cm^2	Ampere per centimeter square
nm	Nano meter

MEMS	Micro-Electro-Mechanical Systems
NEMS	Nano-Electro-Mechanical Systems
IC	Integrated circuit
RF	Radio Frequency
CPU	Central Processing Unit
pJ	Pico Joule
Kbit/kB	Kilo bit
MB/MBit	Mega Bit
μm	micrometer
F	Farad
DC	Direct Current
°C	Degree Centigrade
°K	Degree Kelvin

CHAPTER – 1
INTRODUCTION

The chapter presents an introduction to the challenges the electronic industry is facing and mitigation through the newly understood and practically realized fourth passive fundamental component the Memristor. The application of the technology is resistive random access memory – ReRAM and as an artificial synapse, pointing to few important and urgent need of electronics industry. The advantages over the conventional memories are very high operating speed and density, long term storage without the need of power supply. The challenges are multi treaded. Brief on memristor, its impact on electronic industry and applications is detailed.

1.1 Introduction to Memristor

Moore's law is dying

Physicist Richard Feynman at the annual American Physical Society's meeting on December 29, 1959 delivered a lecture by the topic "There's Plenty of Room at the Bottom" [1]. Idea was to look into the opportunity of straight exploitation of individual atoms as a more powerful form of research. He emphasized on the process which provide the ability to the tools to precisely manipulate elements at molecular and atomic levels. The process enumerated developing of precise smaller dimension tools from a set of relatively larger precise tools to achieve the scaling and manipulation to the required dimensions. He alerted that the scaling issues will open up the frontiers for new challenges in which the role of gravity will reduce and the factors like surface tension [2] and Van der Waals attraction [3] would become more important mainly owing to the dimensions at which the work takes place.

Gordon Moore, co-founder of Fairchild Semiconductor & Intel, through his paper [4] hypothesized doubling components per year per integrated circuit. The forecast was revised by Intel executive David House to doubling every 2 years but is

generally quoted as 18 months. These predictions proved to be the guiding principles for long time plan, to lay down targets and for investigation based development. ITRS [5] International Technology Roadmap for Semiconductors reported slowing of growth rates by 2013 and Moore predicted saturation by 2015 and death of the law by 2025 mainly because scaling was thought not to continue forever. The restraining parameters amongst others are electron tunneling all the way through short channels, passive power dissipation, leakage current through thin insulator film, short channel effects, and variations in device composition and doping. Also, Moore's law is facing challenge from data processing front which requires biological level scaling and circuit density – the primary need for big data processing and artificial intelligence where there are enormously big data sets to analyze. The awareness of impending limits of scaling has motivated a global endeavor to build up alternative/substitute device technologies coined "Technology beyond Moore's law".

In the year 1971 Prof. Dr. Leon Chua of UC Berkeley hypothesized presence of fourth fundamental/elementary element by the name 'Memristor" owing to its property of remembering the previous state in form of resistance – **MEM**ory **R**es**ISTOR** [6]. Memristive effects are visible and relevant at nano-scale where dynamical properties of ions and electrons strongly depend of the system's history in certain time scales [7]. This provides much needed respite to the Moore law's existence. Owing to memristor's unique property to remember its previous state and this effect being prevalent at nano scale makes it very useful especially in the area of non-volatile memory wherein it consumes negligible power moreover requires very little space [8] from fabrication view point on the integrated circuit compared to all other existing memories. Also, memristor's second very important property is its behavior like a synapse of brain [9]. This property has very high potential applications in the area of artificial intelligence and computing, robotic engineering, neuromorphic computing in form of memristor based neuromorphic microprocessor integrated circuits [10, 11].

Other three well known and highly studied fundamental elements are the Resistor (***R***), the Capacitor (***C***), and the Inductor (***L***). All electronics was built using these three fundamental devices. Apart from these the fourth device being used extensively is transistor, an important invention, though it cannot be said to be a fundamental device because one can write its equivalent circuit comprising of resistances and couple of sources of energy using Thevenin's and Norton's theorems.

Memristor is a fourth fundamental passive device. Professor Leon Chau at University of California, Berkeley and Albert Einstein's [12] work were similar in significance but in different fields. Basically Chua was a mathematician and first to put non-linear circuit theory on a solid mathematical groundwork. He thoughtfully is said to be the father of non-linear circuit theory.

He observed the three passive fundamental elements the Resistor (***R***), Capacitor (***C***) and Inductor (***L***) were electrically well defined through the variables voltage ($\boldsymbol{v}$), current ($\boldsymbol{i}$), charge ($\boldsymbol{q}$) and flux ($\boldsymbol{\phi}$). However, from symmetry aspect he noticed the missing link amid the variables the charge ($\boldsymbol{q}$) and the flux ($\boldsymbol{\phi}$). He also noticed that the number of equations relating the variables voltage ($\boldsymbol{v}$), current ($\boldsymbol{i}$), charge ($\boldsymbol{q}$) and flux ($\boldsymbol{\phi}$) inclusive of omitted link to have had been six and through these observations he postulated the fourth passive fundamental element to be the association between the charge ($\boldsymbol{q}$) and flux ($\boldsymbol{\phi}$) and named it Memristor based on its observed fundamental characteristics or the fingerprint.

In Fig. 1.1, the variables are related as per the equation

$$v = \frac{d\varphi}{dt} \qquad (1.1)$$

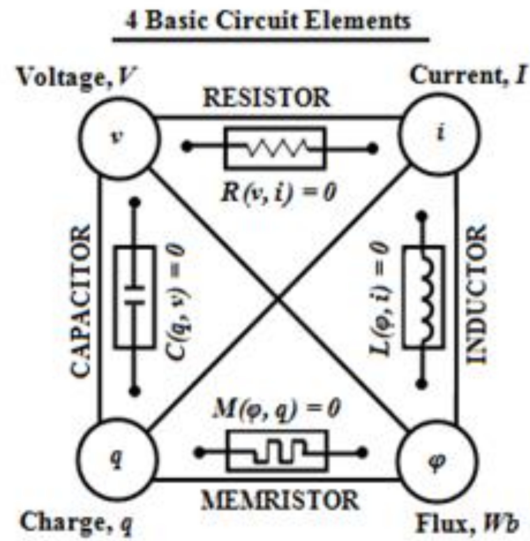


Fig. 1.1 Fourth fundamental element Memristor & equations relating the variables

$$i = \frac{dq}{dt} \quad (1.2)$$

$$q \triangleq \int_{-\infty}^{t} i(\tau)d\tau \quad (1.3)$$

$$\varphi \triangleq \int_{-\infty}^{t} v(\tau)d\tau \quad (1.4)$$

$$dv = Rdi \quad (1.5)$$

$$dq = Cdv \quad (1.6)$$

$$d\varphi = Ldi \quad (1.7)$$

$$d\varphi = Mdq \quad (1.8)$$

$$d\varphi = Vdt \quad (1.9)$$

$$dq = idt \quad (1.10)$$

In equation 1.1 to 1.10

v = voltage

φ = flux

i = current

q = charge

t = time

τ = small time period

R = Resistance

C = Capacitance

L = Inductor

M = Memristor

After publication of the paper [6] the research community put in efforts to find the element but they were not able to figure out the physics which may couple charge ($\boldsymbol{q}$) and flux ($\boldsymbol{\phi}$) because the cause was absent from the equation. It only said things were related to each other. If the cause i.e., physical interaction would have had been identified, then it would have made the equation true and resulted in a real world memristor.

Steve Kang [13] interpreted the cause – A passive device with a state. By this he meant existence of memory in a memristor and that this memory is represented by state variables. So, complete characterization of memristor requires not 1 but 2 equations as follows

$$v = R(w)I \qquad (1.11)$$

Quasi-static conduction relation between voltage & current i.e., Resistance in the equation depends on device's state at that instance of time.

$$dw/dt = f(t) \qquad (1.12)$$

Equation is time dependent in which state variable (w) evolves with time.

1.1.1 Inferences

The inferences drawn are based on eq. (1.1) and eq. (1.2)

- Mathematical modeling of memristor requires two equations.
- These equations don't say anything about flux.
- Any system which has a state which evolves with time is a memristor.
- These equations suggest memristor having an I-V curve as shown in Fig. 1.2.

Fig. 1.2 (a) presents the graph by Leon Chua depicting behavior of hypothetical memristor. Fig. 1.2 (b) presents the graph of experimental behavior of HP Labs memristor devised by R. Stanley William.

Loops match transitional/switching behavior of memristor. It starts with high resistance and current slowly increases with increasing voltage. With increases in the flow of the charge all the way through the device the resistance gradually falls leading to rapid increase in current flow associated with rising voltage till the maximum limit is achieved.

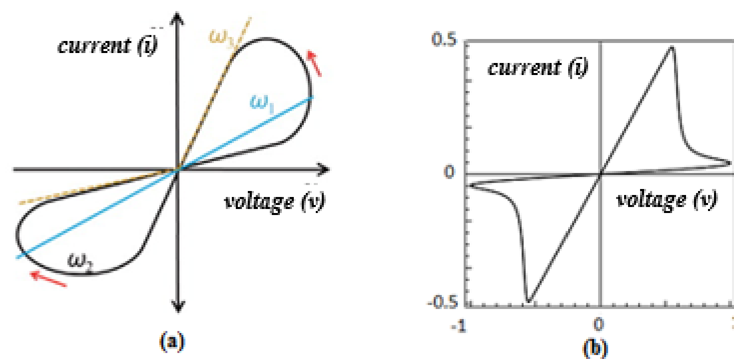


Fig. 1.2 The Memristor *V-I* characteristics representation by
(a) Leon Chua (b) HP Labs

Current decreases but at a low pace with decreasing voltage, because the charge is still flowing through the memristor while the resistance is reducing/dropping resulting in an on-switching loop. Upon reversing the polarity of the voltage the memristor's resistance increases and the resulting characteristics can be termed as off-switching loop.

The *V-I* characteristics look like a bow tie [8]. Chua *et al.* in his paper [6] named these *V-I* curves as pinched hysteresis loop and suggested if the output of an experiment resembles the pinched hysteresis loop then one may be have probably found a memristor. In Fig. 1.2 it can be seen that for any single value of voltage

there are two values of resistance one while the voltage is raising and the other when the voltage is decreasing.

Memristor is fundamental device and it can be said so owing to following reasons:

- Memristor's finger print i.e., *V-I* characteristics cannot be reproduced by any circuit combination involving resistor, capacitor and inductor.
- By resistor it means not only linear devices but devices like diodes, tunnel junctions that have *V-I* characteristics like a hysteresis loop into it.

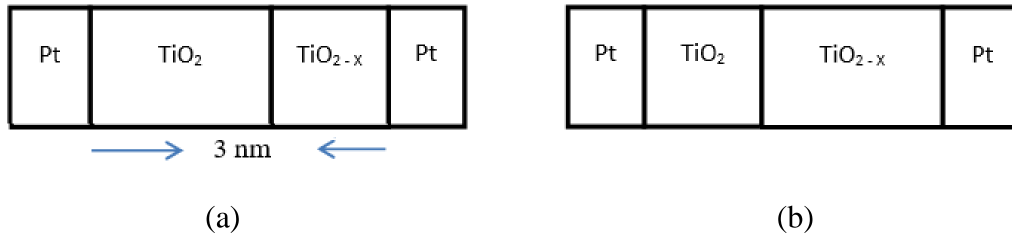
About a decade before a memristor was practically realized at HP Labs [8, 14, 15] a team was constituted by David Packard under the mentorship of R William Stanley with the objectives to

- Return knowledge to benefit of fundamental sciences
- To benefit from technological innovations from a long term project.

This was a long term project and R William Stanley decided to start with Moore's law keeping in mind the realization that the law is facing challenges, and may die eventually mainly owing to further transistor size reduction incapability. After six years into research and working upon the idea of implementing Kuekes Teramac supercomputer on crossbar architecture along with others, Greg Snider co-worker introduced the paper [6] to R William Stanley's team with the intention realize device depicted in the paper. The team was successful in the year 2008.

1.2 HP TiO_2 Bipolar Switch

Fig.1.3 (a) presents that oxide has a highly resistive TiO_2 region and a conductive TiO_{2-X} region. Conductance is owing to high doping of oxygen vacancies which are positively charged. Fig.1.3 (b) upon application of positive voltage to electrode on the right, the positively charged oxygen vacancies drift to left narrowing the tunneling gap.



(a) (b)

Fig. 1.3 Variation of resistance of memristor

The variations within memristor are as follows:

- Memristor physical construction constitutes of two Pt (Platinum) electrodes on each sides and thin film TiO_2 in the center.
- Auto doped TiO_2 behaves like wide band gap semiconductor.
- If slight amount of oxygen is taken away of TiO_2 it results in *n*-type doping. Oxygen vacancies left inside TiO_2 are positive.
- These vacancies are to some extent mobile.
- Under the influence of large electric field the positive charged vacancies drifts and narrows tunneling gap which reduces the resistance of system. The reverse process increases the resistance i.e., the process is reversible. It resulted in a switching device using voltage that gives pinched hysteresis loop.

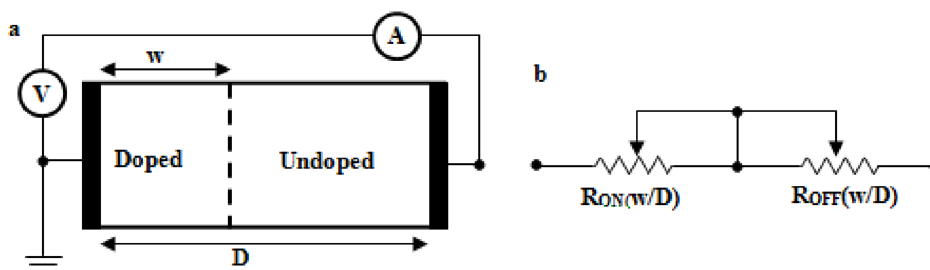
1.2.1 Analysis of HP Memristor

Fig. 1.4 below constitutes of

(a) Representation of the model

(b) Circuit equivalent of model

(c) Simulation outcome depicting ionic drift which is nonlinear in nature



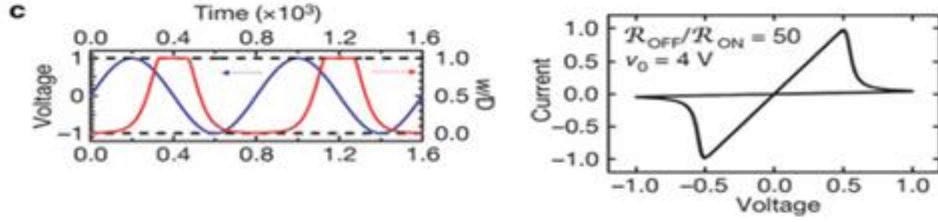


Fig. 1.4 (a) Representation of memristor model (b) Circuit equivalent of (a)
(c) Simulation results [8]

Blue waveform indicates the voltage as stimulus and red waveform indicates time reliant analogous change in normalized state variable – (w/D) and (c) represents *V-I* characteristics of the memristor. To obtain the equations governing the working of memristor the following points need to be taken into consideration

- There are 2 variable resistances in series with each other.
- One resistance is representing TiO_2 when it is stoichiometric
- Second resistance when it has oxygen vacancies into it
- When we push or pull the dividing line or the end state between the oxygen vacancies and stoichiometric TiO_2 then one can vary the resistance of total device.

Above points results in the following equations

$$\text{Ionic drift} = \frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \quad (1.13)$$

Speed of dividing line i.e., drift is equivalent to electric field times the current

$$\text{Electronic current} = v(t) = \left[R_{ON} \frac{\omega(t)}{dt} + R_{OFF}\left(1 - \frac{\omega(t)}{D}\right)\right] i(t) \quad (1.14)$$

Voltage is function of current and resistance dependent on the state variable

Eq. (1.33) and eq. (1.14) are the equations written down by Leon Chua to define a memristor and the HP Labs device is actually a memristor. These equations result into the equation for memristance as follows:

$$\text{Memristance} = M(q) = R_{OFF}\left[1 - \frac{\mu_v}{D^2} R_{ON}\, q(t)\right] \quad (1.15)$$

From above equations, it can be seen that linear conduction and linear drift has a term which is inversely related to the width of the device that is = $1/_{D^2}$ meaning memristance is 1 million times more significant at nanometer scale than at micron scale and unobservable at millimeter range. HP Labs demonstration of working of memristor is depicted in Fig. 1.5.

Crossbar Architecture: A mesh constituted of perpendicular wires forms crossbar architecture. A switch is a junction formalized by two perpendicular wires crossing each other. It opens and closes upon application of reversible voltage across two wires connecting it.

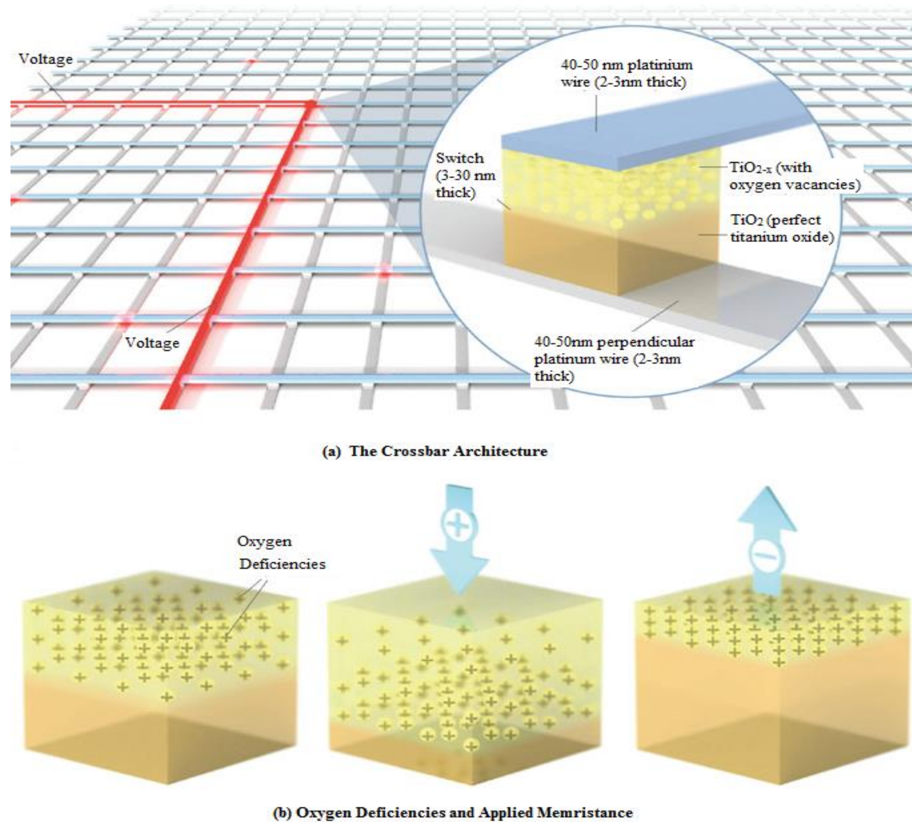


Fig. 1.5. (a) The Crossbar Architecture
(b) Oxygen deficiencies and Applied Memristance

The Switch: A switch is formed by two layers of titanium dioxide (TiO_2), having dimension of 40 nm, with a perfect ratio of 1:2 of titanium to oxygen in lower TiO_2 layer, thereby creating an insulator. In the same lines, the upper TiO_2 layer is deficient of 0.5 percent of oxygen and goes by the nomenclature TiO_{2-x}. This deficiency of oxygen vacancies makes the layer conductive and metallic in nature.

Oxygen Vacancies and Applied Memristance: The analogy also depicts the deficiencies (TiO_{2-x}) as "bubbles" spread all through the upper layer. The deficiency of oxygen (TiO_{2-x}) which is positive in nature is pushed or repelled below to the TiO_2 layer upon application of a positive voltage to the switch. It manifests in physical lowering of the boundary and increase in the total conducting region of the switch. The conductivity of the switch can be controlled by varying the intensity of the applied positive voltage across the switch.

On the contrary TiO_{2-x}, i.e., oxygen vacancies represented as positively charged bubbles, are pulled out of TiO_2 upon application of a negative voltage thereby increasing the overall resistivity and amount of insulating TiO_2 in the switch. The conductivity reduces with magnitude of negative voltage. Memristance comes into existence in the said switch when the oxygen bubbles remain positioned upon removing the applied voltage across the switch. This freezes the boundary meaning remembrance of magnitude of last applied voltage.

1.2.2 Memristor Reported as Anomaly

The working of memristor allows understanding of enormous literature that reported manufacturing of nanoscale devices or circuits which had *V-I* characteristics similar to that of a memristor well before Leon Chua published his semantic paper – The missing memristor found.

Researchers were publishing papers which showed pinched hysteresis loop but were unaware of their findings, as listed in Table 1.1, and reported it as anomalous

resistance, capacitance, inductance or something strange, but all the time they were referring to a memristive behavior. Memory effects were prevalent prior to officially understanding the memristor.

They missed upon the fact because of the following reasons [8, 13, 14]

- At nano-scale a small voltage of about 2 volts generates a very high field and this field is sufficient to cause the atoms to move.
- Wherever there is existence of coupled movement of electrons and atoms in a device it results in a memristance.
- Whenever above two points were satisfied they were finding memristance but they tried to define the device using resistor, capacitor and inductor.
- Gap in analysis – Defining memristor requires two equations i.e., eq. (1.11) and eq. (1.12), for complete characterization.

Table. 1.1 Summary of memristive effects in different materials.

Sr. No	Author	Material
1	S Seo *et al.* (2003) [16]	Ni
2	B J Choi *et al.* (2005) [17]	Ti
3	H Sim *et al.* (2005) [18]	Nb
4	E. Tabachnikova *et al.* (2008) [19]	Zr
5	A Chen *et al.* (2005) [20]	Cu
6	M Kund *et al.* (2005) [21]	Ag
7	Y. You *et al.* (2006) [22]	Nb
8	N Banno *et al.* (2006) [23]	Cu(S)
9	T N Fang *et al.* (2007) [24]	Cu
10	C Park *et al.* (2007) [25]	Ni
11	W Guan *et al.* (2008) [26]	Zr
12	Y Nishi *et al.* (2007) [27]	Cu(S)
13	S. Mojarad *et al.* (2007) [28]	Ni

It can be said that the memory effect is all prevalent in nature and is independent of type of material being considered. It has prominence at nano-scale, which relates the dynamic properties of electrons and ions that show dependency on history of the system. This history dependent property is resistive in nature, indicating memory effect, and falls in the memristive domain. The properties to investigate are physical mechanisms resulting in memristive effect, classification of memristive physical mechanism, and investigation of operating voltage, current and power of various memristors so that proper choice of material for application in question can be reached to.

1.2.3 Analysis of Memristor for its Physical Behavior

Through proper experimental set-up quasi-static conduction mechanism of memristor can be controlled and dynamical evolution of state can be made possible. Here the state is the drift which produces the dividing line between R_{ON} and R_{OFF}. Hence, we can infer that we have very fast switching at nanosecond and simultaneously infinite life time.

- <u>Reason for Switching of Memristor</u>

  Drift velocity's dependence on electric field is exponentially in nature in accordance classical Einstein relationship

  $$\frac{D}{\mu} = \frac{kT}{q} \qquad (1.16)$$

  Here:

  D = Diffusion coefficient

  μ = Charge carrier

  k = Boltzmann's constant

  T = Temperature

  q = Elementary charge

The exponential is huge which results in 20 orders of magnitude of change in drift velocity – 1 m/sec, when the field is varied by a very small amount, say 2V in this

high field regime in nanometers. Drift results in change of position of state variable (w) of dividing line between R_{ON} and R_{OFF} and hence the state of the device.

- Memristor as Memory Owing to Infinite Life Time

  After switching off the voltage the ageing diverges to virtually infinite life time. This indicates applications of memristor to be nonvolatile memory and as synapse thereby opening the area of study on ultra high density nonvolatile memory and neuromorphic hardware.

1.2.4 Implications of Memristor

- Preservation of Moore's law
- Initiation of worldwide effort to search and develop alternative device technologies
- New device characteristics indicates new applications and opening up of research and development work
- Initiation of broad spectrum study to understand the impact on existing technology
- Identify and generate the areas of application of technology

1.3 Motivation and Need

The memristor has several applications as enumerated

- Hybrid circuits using combination of memristor and transistor [29].
- Memristor as ultra high density nonvolatile memory as replacement to DRAM and FLASH memory [30].
- New devices like FPGA chips with n-X times density and speeds at low power consumption.
- Analog neuromorphic computer [31] i.e., non-Boolean logic without simulation indicating real time computations.
- Optical computer system [32].

- Company named ‘KNOWM’ initiated research on memristive based deep learning [33].

Memristor as a disruptive technology will effect following areas

- Reconfigurable logic in which about 7.9 trillion/second the numbers of transistor manufactured globally for the purpose. Here, memristor become low-end disruptive technology due to yields, endurance, fabrication processing, compatibility, incumbent risk aversion and related issues.
- Synapse for which 5 quadrillion/second transistors manufactured. This presents a big opportunity for new market disruption owing to ultra-efficient hardware.
- Existing EDA tools will need complete overhauling to produce the results for memristive based devices and applications.
- Existing standards and protocols will require major change.

1.3.1 Resistive Random Access Memory (ReRAM)

ReRAM suffices sufficient potential to present itself as a next age nonvolatile random access memory with significant advantages over the conventional memories being used currently [34]. Materials displaying switchable/variable resistance and functioning as a storage media is the most noteworthy element for the performance of the memory. Hence, material study is the integral part of the technology.

Advantages offered by ReRAM

- Higher speed
- Denser memories
- Long term storage
- Exceptional scalability
- Very low power usage
- Economical

- No requirement of exterior power supply to keep up/preserve stored information.
- Good CMOS compatibility crucial for realistic applications and mass manufacture.
- Simple structure

Challenges to ReRAM *[35]*

- Materials problem
- Reset/Set (R/S) Mechanism
- Manufacturing issues
- Integration issues
- Function of computational materials discipline to devise novel ReRAM.

The resistance switch mechanism is akin to structural or phase changeover in science of materials which is associated to various defects like

- Point defects
- Linear defects
- Planer defects

Classification of Reset/Set Mechanism *[36]*

- Electronic scale (trapping/detrapping of carriers)
- Atomic scale (migration of point defects)
- Apparent change of atomic structure (Metal-Insulator transition)
- Clear change of micro composition (Thermo-Chemical reaction)
- Complex mechanism (correlation between mechanisms like metallic and hopping conduction)

Fig. 1.6 represents simple ReRAM structure and presents an apparent correlation between the property of the material and performance of the device. Dissimilarity in material structure results into distinct resistive values and corresponds to two

logic states in case of binary system and into multiple states in case of multilevel logic system. Dissimilarity in material structure can be due to electronic or atomic change at micro and even nano scale. Two structures depicted as Structure 0 and Structure 1, possesses different energy level as depicted in Fig. 1.7. In presence of electric field few materials behave as resistive switch which fundamentally is a changeover amid two structures/phases.

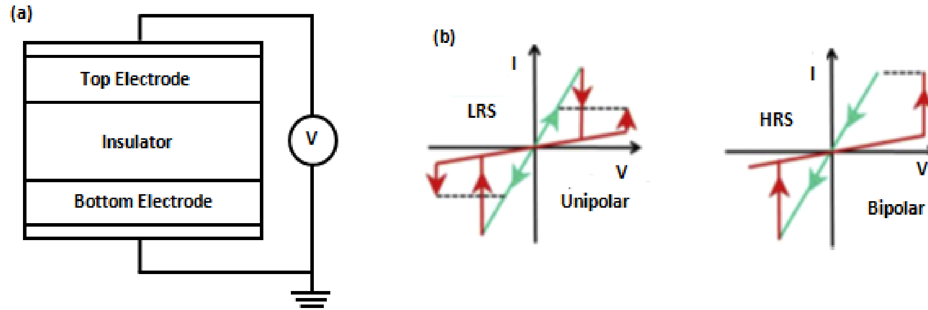


Fig. 1.6 (a) Simple ReRAM structure (b) *V-I* curves representing unipolar and bipolar switch mode

It also depicts the structural resistance switch phenomenon. As a appropriate material for ReRAM, the values of the parameters *"D"*, "E_{set}", "E_{reset}", "E_{diff}" and *"R"* ought to be reasonably small to achieve the properties like high endurance, less power use and enhanced speed of operation. However, too little values of *"Eset"* and *"Ereset"* may weaken the preservation of the memory.

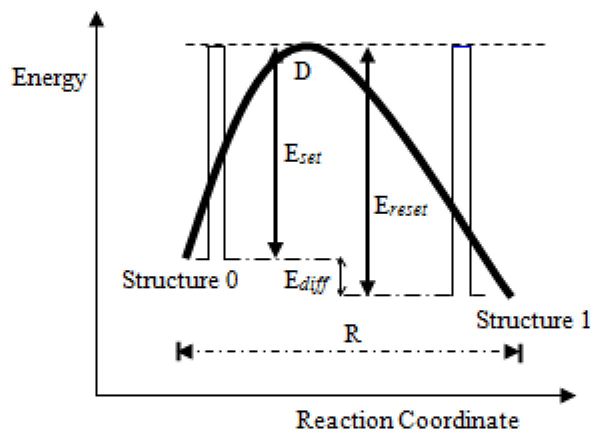


Fig. 1.7 Illustration of energy profile between two structures of material as an analogy to R/S process in ReRAM

Two vertical columns represent energy required to be supplied by electric pulse.

D - Reproducibility and fidelity of transition path, similar to endurance, equivalence and reliability of Re RAM

E_{set} - Energy required for transition from structure 0 to structure 1,

E_{reset} - Energy required for transition from structure 1 to structure 0,

E_{diff} - Dissimilarity in energy of the two states

R - Displacement of any ions/electrons in Reset/Set procedure, correspondence is with operation time

E_{set} & E_{reset} - Related to retention of ReRAM

First investigational study of R/S was carried out more than fifty years ago. In 1962, Hickmott [37] was successful in investigating a huge negative resistance in the *V-I* characteristics of few oxide films namely: TiO2, ZrO2, Ta2O5, SiOx and Al_2O_3. The exigency to discover the substitute of Flash memory boosted the inquiry for R/S occurrence in new materials, principally in the past few decades. Diverse materials have exhibited the R/S phenomenon, that are segregated into ternary, binary and new multifaceted oxides, nitrides, chalcogenides, unstructured carbon, and a few natural organic material through explicit use in flexible electronic applications. Switching performance of these materials is gauged on the parameters like mode of switching, speed of operation, endurance, etc. Binary oxides have been expansively studied owing to the ease of fabrication process using these materials with good agreement on crucial parameters and performance.

Table 1.2 shows periodic table describing the candidate materials for ReRAM

- Binary oxide composition.
- Metallic elements (used as host by these oxides) to study as R/S materials.

Table 1.2 Periodic table with highlighted host metals of ReRAM

1A																	0
1 H	IIA	30 Zn +2 A/C Y/N — Host metallic element; The microstructures of the oxides (C = Crystalline and A = Amorphous); Nominal valance state; Whether electrodes are involved in Reset/Set Process										IIIA	IVA	VA	VIA	VIIA	2 He
3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
11 Na	**12 Mg +2 C N**	IIIB	IVB	VB	VIB	VIIB	VIIIB			IB	IIB	**13 Al +3 C N**	**14 Si +4 A Y**	15 P	16 S	17 Cl	18 Ar
19 K	20 Ca	21 Sc	**21 Ti +4 C/A N**	**23 V +3/4/5 A N**	**24 Cr +3 C N**	**25 Mn +2/3/4 C N**	**26 Fe +3 C N**	**27 Co +2/3 C N**	**28 Ni +2 C N**	**29 Cu +1/2 C N**	**30 Zn +2 C N**	**31 Ga +3 A N**	**32 Ge +4 C Y**	33 As	34 Se	35 Br	36 Kr
37 Rb	38 Sr	**39 Y +3 A N**	**40 Zr +4 C/A N**	**41 Nb +3/4/5 C N**	**42 Mo +6 C N**	43 Te	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	**50 Sn +4 C N**	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba	**57 La +3 C N**	**72 Hf +4 C/A N**	**73 Ta +3/4/5 C/AN**	**74 W +6 C Y**	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 TI	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra	89 Ac	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Uub						

- Metallic elements nominal valence state.
- Oxide’s microstructure to amorphous or crystalline.
- Direct involvement of electrodes in the RS process.
- RS layers being hetero-structures constituting of many oxide thereby totaling up to degrees of autonomy for selection of material..
- Thoroughly studies binary oxides.
- Space for future study on materials not yet examined.

1.4 Thesis Organization

The thesis work compiles the complete work in seven chapters.

Chapter – 1: The chapter explains the challenges being faced by the electronics engineering discipline and its effect, concept of fourth fundamental passive component the memristor, its working principle and applications areas: ultra-high density nonvolatile memory and as a synapse of a brain, motivation to work on memristor. The thesis organization is discussed at the end of the chapter.

Chapter – 2: The chapter discusses the literature survey carried out with the help of different research papers in the field of memristor and its application as very high density memory applications based on reversible phase change of material from crystalline to amorphous and metal to insulator. The literature gap has been identified and the problems formalized by defining the problem statement, and research objectives.

Chapter – 3: This chapter describes nonvolatile Phase Change Memory (PCM) Cell and Metal Insulator (M-I) Phase Change memory cell. It describes memory effect, characteristics and switching mechanism in phase change material. Further the different materials are reviewed for switching mechanisms and are classified in accordance. The PCM & M-I cell structure and SPICE programming concepts are

detailed. The chapter includes the complete description and assumptions in detail to support the cause related for devising new and reliable memory.

Chapter – 4: The chapter explains the methodology and tools for simulation of PCM & M-I memory cells. The need for simulation is described with related advantages. The chapter also discussed the different software tools description form simulation as well as synthesis

Chapter – 5: The chapter explains the SPICE simulation of Phase Change and Metal-Insulator transition memory cells. The simulation results of the same are presented.

Chapter – 6: The chapter details about simulation and design outcomes in digital domain with respect to PCM cell and array. Also, described is the simulation and synthesis result of the adaptive algorithm for the PCM array and its realization in form of a FPGA chip. Verification of the functionality of the synthesized chip was carried out through an experimental set up that used Virtex-5 FPGA for synthesis purpose which was further supported by Xilinx Integrated System Environment (ISE). It enumerates and provides the procedure to mitigate the issues related with non-binary storage of information in the memory cell. It is a central and vital reason responsible for reducing the total per bit cost thereby escalating the competitiveness of PCM cell technology in nonvolatile memory market segment.

Chapter – 7: The chapter includes the conclusions drawn from the research work and recommendations about the further research and possibilities.

CHAPTER – 2

LITERATURE SURVEY

The chapter discusses the literature survey carried out with the help of different research papers in the field of memristor and its application as very high density memory applications based on reversible phase change of material from crystalline to amorphous and metal to insulator. The literature gap has been identified and the problems formalized.

2.1 About Memristive System

Dr. Leon Chua *et al.* [6] was successful in establishing independent existence of memristive systems through its exhaustive study and presentation of the phenomenon. He defined the system's *V-I* characteristics to a hysteretic curve and called it memristive fingerprint. Hence, any system or device that establishes this fingerprint is said to be a memristive device. However, prior to Chua fitting in the memristive phenomenon in perspective the contribution knowingly and unknowingly, in the same area by other people has been reviewed below.

Hodgkin and Huxley *et al.* [38] identified and related ionic systems to membranes in neuron cells (of a Loligo). They related the change in flow of current with the change in potential but all the while, they were associating depolarization of giant axon of Lilago with abrupt change/displacement potential of the membrane from its position of rest. They also presented facts related to the reverse condition potential of the membrane normalizes/restores back all of a sudden. They divided the experiments in two parts

- The period wherein depolarization is small/brief compared nerve time scale.
- The phase wherein the depolarization is comparatively elongated.

The initial part of the experiment demonstrates activities related to movement of sodium ions while the later part shows movements related to ions of potassium.

Sapoff and Oppenhiem *et al.* [39] identified and related resistive behavior of thermistors to memristive systems.

Argall *et al.* [40] defined switching between three distinct conductive states of thin film anodized TiO_2. Linked the characteristics of these three states to temperature range between 4.2°K and 500°K and emphasized on the fact that dielectric's phase change not being responsible for reversible switching.

Hickmott *et al.* [37] initiated research in the area of memristive systems by observing hysteretic behavior in oxide insulators. He prepared Metal-Oxide-Metal sandwich by the process of evaporation of films of metals and observed *V-I* characteristics which displayed large current densities and negative resistance.

Table 2.1 Properties of resistive switch

• Prepared Metal-Oxide-Metal sandwich by process of evaporation of films of metals126 • Observed *V-I* characteristics which displayed ▪ Large current densities ▪ Negative resistance
• Systems Studied and parameters observed are as tabulated: ▪ Ti-TiO_2-Au, Al-Al_2O_3-Au, Al-SiO-Au, Ta-Ta_2O_5-Au, Zr-ZrO_2-Au. ▪ The observed respective voltage of the system at maximum current were ▪ 3.1V, 2.9V, 2.2V, 2.1V and 1.7 V at peak value ratio of 30:1 with maximum, minimum and average current densities were mapped to 10, 25 and 0.01 A/cm^2 respectively.

Simmons and Verderber *et al.* [41] demonstrated resistance switching within thin films of silicon monoxide (SiO) sandwiched amid electrodes of metal.

Observations

- Noticeable quantity of current being drawn from one of the electrodes of thin film insulators, produced by electrolytic introduction of gold ions from one electrode.
- Conductivity was dependent on temperature
- Negative resistance was controllable by voltage
- Displayed hysteretic curve i.e., voltage was reversible in nature
- Memory effect were governed by thermal voltage

Postulations

- Introduction of broad band localized impurity levels in forbidden band of insulator by injected ions.
- Tunnelling of electrons through insulator amid adjoining sites in impurity band
- Trapping of electrons in impurity band under specific circumstances

Kang *et al.* [13] systematically generalized of the memristive theory to a category of dynamic nonlinear memristive system, by identifying memristive behavior and varying physical mechanisms in numerous systems. The memristive mechanisms reached to were thermal, chemical, ionic, spin polarization, phase transitions and others. He clarified that these devices behaved like a dynamically characterized resistor possessing memory and inductive as well capacitive effects capable of discharging energy, by not producing phase shift between the input and output providing it the zero crossing property thereby producing the *V-I* characteristics resembling the hysteretic curve. He elaborated the hysteretic fingerprint of the device to be frequency dependent, in which it behaved linearly at small frequencies and nonlinearly at elevated frequencies, and the fact which created confusion in identification of numerous devices working on memristive principles.

Strukov *et al.* [42] recognized resistive switching devices as memristive systems.

He was first to build foundations of understanding and to demonstrate through analytical examples about the natural occurrence of memristance in various systems at nano-scale. The reason exemplified was coupling of ionic and solid-state electronic transport under the influence of an external bias voltage.

Pershin and Di Ventra [43] identified and related spintronic devices to memristive systems with convenient control compared to ionic transport based systems. He also analyzed time-dependent spin transport at semiconductor/ferromagnet junction, resulting in broadening the range of semiconductor spintronics applications.

Driscoll *et al.* [44] identified and related polaronic systems to memristive system using Vanadium Dioxide VO2 at room temperature. The current, electric field and photo-excitation controllable reversible phase transition is between Metal and Insulator.

Wang *et al.* [45] identified and related phase-transition materials to memristive system. Identified properties of phase change memories illustrated below, making it a first choice of the industry.

- Non-volatile
- High density
- High contrast
- High cycling
- Low power-consumption
- Capable of changing memory states with low current
- Capability to store data in digital format without accumulation of electric charge

Hoefflinger, B. *et al.* [46] segregated memory devices into important categories/segments as enumerated:

- Nano-ionic
- Nano-thermal

- Macro-molecular memory
- Memory devices based on molecular effects

2.2 Switching in Resistive Memory Cells

Bipolar resistance switching

Both negative, positive reversible polarities of voltage are essential for switching a device from high resistance status to low resistance condition and back when switching is bipolar in nature. Fig.2.1 shows generalized form of *V-I* curvature for bipolar resistance switching. Measurements of practical curves will naturally be different from the one depicted in the figure owing to the conditions prevailing during measurement and type of system being used for experimentation purpose. Bipolar hysteretic loops are threshold dependent in which a relatively significant potential difference is required to bring the change of the status i.e., resistance of the device. However, low potential differences do not bring about the resistive change in the status of the device. This is linked with reactions or combinations of reactions like electrochemical and ionic transport. Importantly, the change in the resistance is continuous capable of multiple states/information/bits in a single memory cell.

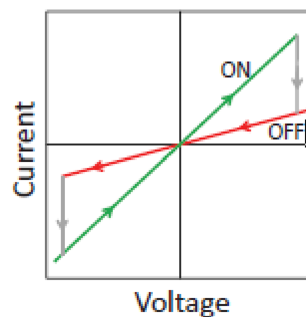


Fig. 2.1 Bipolar switching

Unipolar resistance switching

Thermal effect is considered the reason for unipolar switching. The Set (Off to On) and Reset (On to Off) transition and associated potential difference is shown in Fig. 2.2. In general, the reset voltage is always lower than set voltage. The

electroforming process in the memory cell results in a controlled resistive feeble conducting filament. It is destroyed to a certain degree owing to release of huge quantity of heat during the period of reset process whilst in the reset period it reconstructs back.

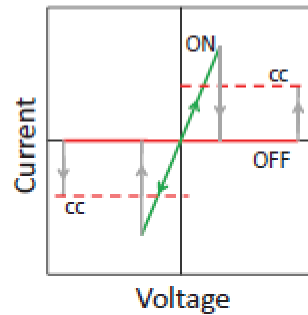


Fig. 2.2 Unipolar switching

Irreversible resistance switching

The resistive change of the state is irreversible and the typical fingerprint of memristive devices i.e., the hysteretic *V-I* loop is not observable or followed by this type of switching as shown in Fig. 2.3. The devices fit into memristive realm only owing to the history dependent resistance change of the device.

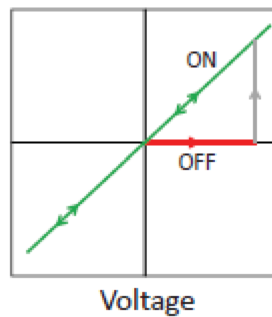


Fig. 2.3 Irreversible switching

2.3 Classification of Phase Change Phenomenon

Reversible crystalline to amorphous phase change memristive system

Phase-change memory cells make use of phase-change materials that are capable of existing in dissimilar phases (minimum of two) i.e., amorphous and crystalline. These phases are characterized by unique physical properties like resistivity, optical reflectivity, etc. The thought of phase change memory (which goes along with various names like PCM, PCRAM, PRAM, Chalcogenide RAM, Ovonic Unified Memory, and CRAM) depends on abilities to electrically induce switching amid amorphous and crystalline states by the Joule heating owing to the flow of current in addition to probe the cell's state by measuring its resistance. Additional energy is not required to store the data because the states are stable.

Metal-Insulator phase transition memristive system

Previously, non-interacting electrons were confidently used to illustrate the dissimilarity among the metals and insulators. Afterwards electron-electron interaction $\left(\frac{e^2}{r_{12}}\right)$ was understood and introduced in to the problem and it was seen that free electron-gas crystallizes at low-densities and the in a low conducting state. One electron atom, cubic crystalline array with lattice parameter d is shown in Fig.2.4. It was observed that for sufficiently large value of 'd' (which allowed tunneling) the array behaved like an insulator and metallic for small values of 'd' indicative of metal-insulator transition with the condition $d > d_o$ the array is insulator and when $d < d_o$ it is a metal.

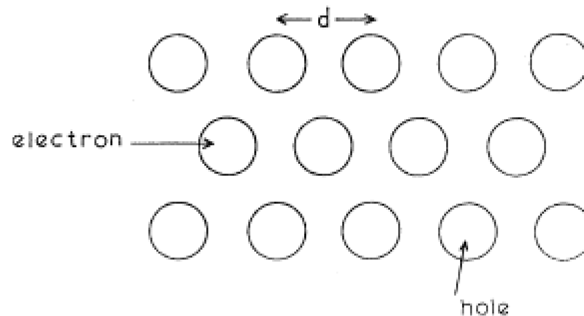


Fig. 2.4 Crystalline array of monovalent atoms

Other memristive systems are as summarized below:

- Spintronic systems:
  Semiconductor & Metallic

Memcapacitive systems

- Memcapacitive systems based on geometry
  MEMS and NEMS, System based on elastic memcapacitance, System based on other geometrical memcapacitance
- Memcapacitive system with delayed response
  Super lattice and Ionic
- Memcapacitive system based on permittivity switching
  Polymer and Phase transition
- Memcapacitive system based on spontaneously polarized medium
  Ferroelectric
- Other memcapacitive systems
  MOS capacitors with nano-crystals

Meminductive systems

- Meminductive system based on Geometrical
  Bimorph
- Meminductive system based on elasticity
  Other meminductive systems and Ionic channels

Other systems with memory

- Devices with three terminals
  Electrochemical cell “memristor”, Solid state “memristor”, Ploymeric transistor and Memristive component in Josephson junctions

Application of memory elements

- **Digital applications**

  Digital memory and Logic

- **Analog applications**

  Neuromorphic circuits and hardware, Quantum computing with memory circuit elements, Learning circuits, Programmable analog circuits, Emulators of memristive, mamcapacitive and meminductive systems.

2.4 Challenges to Moore's Law and Mitigation

Harwick Johnson et. al [47] General Impact of Integrated Circuit Technology

Technology that impacts common man in abundance through its simple uniqueness has the capacity to become the general purpose technology. Paper emphasizes the impact of the Integrated Circuit Technology on the world which has enabled coining of its name – The General Purpose Technology.

The reasons include

- Appeal and simple penetration up to last user of the society
- Acceptance of the technology based products worldwide
- Mass penetration contributes to robust economic growth and generates overall wellness of the society
- Maturity of the technology creates allied technologies and products and related services thereafter.

Jim Magoun et. al [48] Scenario prior to Moore's Law.

The integrated circuit technology has its roots embedded to invention of Thomas Alva Edison's bulb. Fleming observed the Fleming's effect leading to invention of a diode followed by transistors and their versions. The applications were new, powerful and unregulated. Circuits were designed using individual components. It called for stringent technical holds and academic rules and regulations.

- Academic rulings were placed to make available information regarding fundamental science of semiconductor, designs of transistor circuits and its operation, maintenance and modes of transistor application to general public.
- Technical holds included provisions related to circuit miniaturization/smallness, measures for less power consumption and extended reliability in adverse temperatures.
- This lead to major changes like shift
  - From germanium to silicon based devices
  - Invention of monolithic integrated circuit design by Robert Noyce of Fairchild in 1960s leading large scale integration of transistors in single chip possible.

Robert R. Schaller et. al [49] Moore's Law and its Era

Above paper and especially Gordon E Moore provided an opportunity to industry to think about

- Increasing the density of transistors in the integrated circuit
- Lessen the emphasis to improve operating characteristics of individual device.

CMOS technology complemented the Moore's law drive manifold resulting in substantial increase in maturity and stability of IC industry compared to isolated and unreasonable research and development of new applications by directing the energy towards resolving practical issues by incorporating complex circuits. Notable Contributions of Moore's Law

- Nvidia Volta 12nm Graphics Processing Units
- 3D NAND Storage
- Intel Corporation 10nm Process Technology
- Samsung/Qualcomm 10nm Transistor
- IBM Research 5nm Transistors
- Wing River/Intel Corporation Industrial IoT infrastructure
- Berkeley Lab 1nm Carbon Nanotube

Misa T J et. al [50] Roadblocks to Moore's Law

The industry thrived on Moore's law by overlooking the major problems for over half a decade. The issues were dopant clustering and distribution, and electron tunneling through gate oxide leading to issues enumerated below with no solutions in sight.

- Manufacturing
- Reliability
- Yield
- Power supply
- Threshold voltage
- Thermal management
- Performance

Based on relevant parameters available Robert H. Dennard provided the summary of the technology for

- Scaling to dimension
- Voltage
- Scaling

The parameters and challenge to continued scaling were identified to

- Minimum attainable gate oxide thickness
- Interconnect/linking resistance
- Non-scaling of subthreshold slope.

Limitations to Dennard law started to appear in sub-100nm scale. These problems were mainly owing to material shortcoming thereby limiting the performance of the device. They were mitigated temporarily by equivalent scaling which included innovation on a set of materials to achieve Dennard scaling. However, it was not successful beyond a certain time period resulting in increase in cost per transistor – the industry nightmare. Industry tried to mitigate the problem by shifting the focus

on customized IC solutions to cater to markets based majorly on DRAM – Dynamic Random Access Memory and Microprocessor (CPU).

Radojcic et. al. [51] More Moore – Mo(o)re

More Moore i.e., Mo(o)re concept involves maintaining the expected industry standards i.e., doubling of circuit density per 2 years, based on Moore's law. Achievement is based on following four steps

- To improve power/energy performance for individual switching event
- Improvements in frequency of operation
- Improvements in density of transistor in a given area
- Reducing/maintaining cost per transistor based on continuous CMOS evolution.

Methods adopted were

- Iteration of equivalent scaling technology
- Implementation of new device geometry
- Integration of new device materials.

  However, the success was limited.

Faber H et. al. [52] More than Moore

The limited success of Mo(o)re prompted industry to look for option like More than Moore. The industry focused on heterogeneous functionality integration into the CMOS platform using system like

- RF circuits
- Sensors
- MEMS
- FPGA in data centers as accelerators in conjunction with CPU
- Tensor processing units with deep learning applications.

All this catered to specialized needs but offered disadvantages like domain specific applications and innovations leading to the solutions which were not universal in nature.

Shalf J. et. al. [53] **-** Beyond Moore

Technology trends and limitations led ITRS – International Technology Roadmap for Semiconductor to introduce new chapters

- Emerging Research Devices [ERD]
- Nanoelectronics Research Initiatives [NRI]

The goal is to achieve scientific breakthroughs like

- Logic devices for next generation
- Concepts leading to new memory system
- Advance in pattering and key processing steps
- Three Dimensional system integration
- Advanced nano interconnects
- Computing advancements in Artificial Intelligence and Neuromorphic domain
- Quantum computing

Aim is to look for new innovative technologies keeping in mind Beyond Moore concept.

2.5 Memristor, Its Impact and Roadmap

Robert Kozma et. al. [54-55] Are Memristors the Future of AI?

Author emphasizes on the fact that popularity of memristor is due to its applications as super ultra-dense nonvolatile memory and as analog memory generating ideas like instant turn on computers and brain-like machines/neuromorphic architectures respectively. In general memristive technology possesses the potential to revolutionize scientific research and computing for very long time to come. However, it needs to avoid significant challenges which have capacity to hamper

its broad proliferation thereby preventing full realization of its extraordinary potentials. This necessitates 1technology roadmap, with memristor as a central theme, which may serve to avoid time consuming and financially burdening pitfalls. The approach is manifolds and is enumerated:

- Systematic evaluation and elaboration of foundations of memristor theory
- Conduct systematic studies in the area of materials science to identify ideal memristors for different scientific requirements because all materials that exhibit the memristive properties serve as basis for memristive device with first such compound being HP's TiO_2. Investigation of specific features of memristive compounds is necessary since some may be advantageous in some context and of minimal use in other cases/context.
- Memristive components find applications in electrical circuits. It necessitates the need is to address the issues related to constructing electrical circuitries.
- The underlying and essential feature determining the operation of memristors is pinched hysteresis loop. The nonlinearity provides the most important feature extending the use of using the device in continuous operational mode which falls in and as a part of analogous computational paradigm.
- Currently the digital domain is dominant with omnipresent digital computers. It implies the current industry to put all efforts on to manifest digital applications of memristors to garner the profits of digital computing realm to the maximum level.
- Inherent and natural applications
  - Super ultra high-density nonvolatile memory
  - Inherent learning capability enabled design of electronic circuits providing data processing and memory functions computation capability on unified hardware device leading to simplified solutions to complex concepts related to neuromorphic computing and artificial intelligence.
- Memristor is a new component with unique features and requires new CAD simulation expertise and different computing environment.

Deepak Chopra et. al [56] Foundation for Memristor Applications

An average human brain constitute of approximately 100 billion nerve cells or neurons connected with about a trillion to perhaps even a quadrillion connections known as synapses. These are in constant dynamic state of modeling and remodeling in response to input stimulus. Mathematically it indicates about 10 to 10 thousand synaptic connections with a single neuron. These synapses have the ability to learn online in real time. In other words, they have the ability to process the information while passing it on to the neuron as a response to a stimulus. Upon reaching a particular threshold value, the neuron fires, meaning it has evolved and adapted to new information and simultaneously stored it in form of a status which in turn is subject to change when the process repeats at some other instance of time. Memristor is a device which behaves like a synapse.

Memristive nano-devices have huge potential for constructing small power intelligent/clever machines. Their small dimension and dynamics have recommended their utilization as synapses in circuits. The question to explore most effective way to use memristor needs deeper understanding which has been analyzed by various researchers as presented below:

Mead et al. [57] Use of memristor as analog or discrete memory element on digital platform

Onus of popularizing analog computation approach goes to Carver Mead. He proposed the power requirement of 1pJ for floating point computation for subthreshold analog computation.

Arguments Against Digital Approach *[58]*

- Assumption of power requirement through digital approach to reach 10MW to realize human scale intelligence
- Dependence only on nonlinear differential equations as the lone and indispensable mathematical basis to intelligence

- Prediction of CMOS scaling beyond 100nm not being a possibility
- Digital approach to require high 10^4pJ per floating point operation against the postulated prediction of 1pJ for subthreshold analog multiplication.

The above predictions were proven wrong [59] because of the following

- Current digital industry trends indicates scaling reaching below 14nm
- Power requirement per floating point calculation to 5-10pJ range
- Predictions of further reductions in scaling and power requirements
- Importantly, the amount of information computed is 10 bits for analog subthreshold operation compared to 32 or 64 bit results produced by digital floating point operation

Source of Power Loss – Computation Operation versus Parasitic Effect Loss

The dominant power issue owes to parasitic losses occurring due to transmission of information over wires against initial thought being computation power requirement. Avoiding parasitic losses is equivalent to transmitting information without the use of charge, which is not possible. As per the estimation with no architectural enhancements the 10pJ/floating point operation, expected at closing stages of the roadmap, would essentially be littled by the 1000pJ/10000pJ that would be needed to transmit the results and operands between floating point unit and memory subsystem. Comparatively, computational energy cost is too little.

Understanding Parasitic Power Loss: $P = C \times V^2 \times (a \times f)$

Analysis of parasitic power [60] loss requires understanding of working of only one of all basic NMOS gates and the method of power dissipation by it.

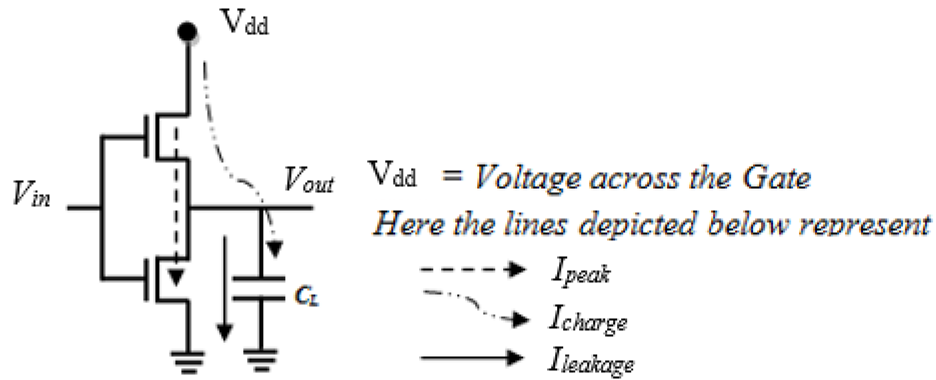


Fig. 2.5 NMOS Gate

For it let us consider the CMOS inverter depicted in the Fig. 2.5 wherein the variables denote the following:

V_{in} = Input voltage of NMOS

V_{out} = Output voltage

V_{dd} = DC voltage supplied to drain of the transistor

I_{peak} = Peak short circuit current through Gate during switching states from 0 to 1 and vice versa

$I_{leakage}$ = Reverse biased Gate Current

C_L = Capacitance of single transistor

t_s = Switching time to transform the state of switch

$f_g = 1/t_g$ = Maximum rate that Gate can cycle at in the processor i.e., Gate's clock frequency

However, the CMOS gate has three current paths

- From the Gate
- Path charging the capacitance of the Gate
- Leakage through reverse biased Gate

$$Energy\ loss\ due\ to\ open\ circuit\ <=\ V_{dd} \times I_{peak} \times t_s \qquad (2.1)$$

$$Energy\ loss\ due\ to\ reverse\ biased\ Gate \sim V_{dd} \times I_{leakage} \times T_g \qquad (2.2)$$

$$Energy\ in\ capacitor\ =\ ½\ \times\ C\ \times\ V^2 \qquad (2.3)$$

$$Energy\ flow\ due\ to\ state\ transition\ =\ ½\ \times\ C_L \times\ {V_{dd}}^2 \qquad (2.4)$$

One cycle has 2 transitions. Full equation depicting loss of energy in one cycle

$$Etr = \left(C_L \times {V_{dd}}^2\right) + \left(2\ \times V_{dd} \times I_{peak} \times t_s\right) + \left(V_{dd} \times I_{leakage} \times T_g\right) \quad (2.5)$$

<u>Significance and analysis of the term $C_L \times Vdd^2$</u>

Gates are switching at processor frequency '*f*' and let 'a' be some constant.

$$Hence\ energy\ output\ of\ a \frac{gate}{sec} \sim C_L\ \times\ {V_{dd}}^2\ \times\ (a\ \times\ f) \qquad (2.6)$$

$There\ are\ about\ a\ billion\ gates\ in\ today's\ microprocessor\ at\ 45nm$
$gate\ technology.$

$$The\ operating\ frequency\ is\ 3\ \times\ 10^9 Hz\ (3\ billion\ Hz) \qquad (2.7)$$

$$Meaning\ generation\ of\ 1\ \times\ 10^9\ \times\ 3\ \times\ 10^9$$
$$=\ 3\ \times\ 10^{18}\ transitions\ per\ second. \qquad (2.8)$$

$$Resulting\ in\ energy\ output\ of\ the\ \frac{processor}{sec}$$
$$=\ C_L\ \times\ {V_{dd}}^2\ \times\ (a\ \times\ f) \times\ (number\ of\ transitors) \quad (2.9)$$

Hence, we can say that effect of short circuit current is the main contributor to the processor's heating apart from the voltage and leakage issues related in smaller junctions. Also, there exists lot of circuit elements that add to the power but are not stringently the logic gates. The discussion indicates major issue essentially being

communication energy produced, regardless of computation mode, i.e., analog or digital.

The methods to mitigate this power issues are as follows:

- CMOS attuned memory which allows close amalgamation of high density memory banks on top of cores to significantly boost bandwidth and lessen $C \times V^2 \times (f)$ losses.
- Photonic interconnect between the chips or within the chip, to make possible energy proficient long distance communication.

Comparison – Analog versus Digital Computation

Analog approach involves hardwiring of critical dynamics related to computational parameters. This involves the risk of dynamics going wrong through missing essential state variables, thereby either reaching to wrong results or no result at all. Also, the approach leads to too simplified models to posses the intended computation ability.

On the other hand, the digital technology [61] is comparatively matured and options like multi-core chips and GPU's – General Processing Units are popular. Combination of digital and software approaches is extensively applied by latest applications like machine vision, robotics and speech recognition. GPU's are essentially popular and works better with prospective multi core chips that will add in denser, on-chip, memory per core to boost bandwidth and lessen power requirements by multiple orders of magnitudes.

2.6 Scope of Memristor

Material property and desirable behavior of the material for Memristor

Internal ion distribution [62, 63] drives the reconfiguration in memristors. Memristor inherently exists at very small dimensions thereby creating even smaller storage levels which are only few nm thick. Alteration in the ionic configuration of

the material is due to the electric field, for sufficient time duration that drives the ionic process which alters the ionic configuration of the material. The process materializes for a moderate voltage drop across the device. Local conductivity changes because of multiple process involving migration and reduction of cations and anions species in the storage level and oxidation. It reflects in the form of annihilation and creation of conductive filament. The occurrence of the process can be either sudden or slow progression involving many different physical processes unfolding at various time scales evolving rich behaviors in a very simple looking structure [64, 65]. The sudden and slow progressions indicates to binary (digital) and analog behavior respectively.

From RRAM – Resistive Random Access Memory perspective the device can be scaled to sub-10nm size and can retain memory state for many years with device properties like long write-erase endurance, sub-nanosecond switching speed and low programming energy in nano-ampere range. Also, the material has the capability to reproduce the properties repeatedly. However, a single material system that combines all the properties simultaneously remains an open challenge. Material and device challenges are summarized as follows:

- Critical issue is that of lowering the programming voltage and current
- CMOS compatibility to provide necessary interface and control operation
- To increase selector performance to minimize sneak currents, device to device and cycle to cycle variability and to raise endurance to bring memristor based computing hardware to real-world applications.

For this these systems need to be scaled up along three axes namely:

- Investigation into aspects related to increasing the size of the functional memristor networks
- To look into improving the system functionality by multitasking in the same hardware system
- Mitigate Memristor – CMOS integration issues for reliable system-level scaling

On-chip memory storage

The general idea is that the computing potential can be enhanced by increasing the computing speed [66]. But closer look highlights the issue of the von Neumann architecture [67], which suffers from throughput problem related to memory access owing to storing of the actual data along with the programming instructions. This leads to processor remaining idle for specific amount of time when memory is being accessed.

This is being mitigated through various methods like:

- Using easily accessible cache to place critical memory
- Multithreading in which multiple operations/processes are managed in a priority based system
- Changing the memory bus design to incorporate parallel processing with the aim to increase the bandwidth/throughput for the memory
- 'Non von Neumann' or 'non von' system modeled around biological world for memory intake based on more distributed principle versus the sequential system popular and prevalent currently.
- To look at new technologies like memristor and use it as a central theme to design architectures.

Biologically inspired computing and Neuromorphic hardware

Cybernetics [68] is a mature and practical thought of application of logic and mathematics to real world problems, the offshoot of which is the bio-inspired computing. However, practical real world leads to paradoxical zone of the universe where there are only probabilities, without surety leading to compromises and statistical resolutions. Contrast calls for efficient methods/methodologies based on combination of thinking, communication and control of either an automatic machine or way of being of a living organism. Realizing the idea requires the entity to possess means of acquisition, use, retention and transmission of information which falls in the domain of self-regulating system. Information processing is always interwoven with cognition.

The notable contribution of the scientists like Norbert Weiner, Claude Shannon [69] and others paved path for evolution of current information age. It helped formation of three pillars of cognitive psychology as follows:

- All that fall in the range from societal activities to neuro-physical mechanisms can be modeled as structured/organized control systems with feed-forward and feed-back loops
- Information theory provides an opportunity to quantify information and entropy thereby theorizing in terms of flow of information
- Statistical theory has the capacity to derive scientific inferences based on the output of controlled experiments for conceptualizing human decision making

These inferences can be transformed into working hardware using memristors, which fits in here, because it has the capability to play a larger role in computing systems beyond memory or storage. This is owing to their capability to be host to – a memory and compute, in same physical device. Memristor based hardware idyllically realizes exceedingly efficient bio-inspired neural networks. Artificial neural networks have outperformed classical systems in processing data intensive and cognitive tasks. Recent advancements in algorithm developments have assisted performance that has surpassed humans in certain specific complex tasks like playing the game Go.

In its simplest structure, a set of neurons linked by weighted synaptic connections form a neural network. Each synapse scaled by the synaptic weight transmits the information from pre-synaptic to the post-synaptic neuron. Typically, the network is trained by updating its synaptic weights to perform a specific task. Modern networks can have multiple (over 100) hidden layers, and thus require training and storage of an enormous number of synaptic connections.

Traditional implementation of neural network is mainly based on conventional computing hardware. The synaptic weights are stored in (off-chip) memory [70]

and requires constant loading into the processing unit for computation to obtain the desired output to pass on to the next neuron resulting in performance limitation owing to von Neumann bottleneck. This method requires huge computing hardware resources and enormous power consumption during the operation.

The memristor-based implementation provides mitigation of the issue in which, a lone device concurrently modulate transmitted signal and store the synaptic weight. A case, in which the transmitted signal i.e., current through the post-neuron, is evaluated by way of the product of the input signal which is the pulse of voltage from the pre-neuron, and the synaptic weight represented by the memristor conductance, via Ohm's law. Same memristor device hosts two operations – compute and memory, thereby eliminating the constant data movement [71] and thus significantly improve the system efficiency.

Additionally, the network structure can be directly mapped into a crossbar form in hardware, where the inputs and outputs are connected to the rows and columns of the memristor crossbar respectively. Furthermore, all inputs can be computed simultaneously in a single read operation, where the output current at a specific column is determined by the summed currents through all the memristors connecting the inputs to the particular column, through Ohm's law and Kirchhoff's law. In other words, a single read operation of an $N \times M$ memristor crossbar with N inputs and M outputs performs an $N \times (N \times M)$ vector-matrix multiplication, obtained naturally through physics. The same task will require $N \times M$ multiply-accumulate operations in a conventional system, highlighting the high degrees of parallelism in the memristor-based approach. The co-location of memory and logic and high level of parallelism are two of the most attractive features that make memristor-based neural network hardware highly efficient. Memristor based hardware is also compatible with online learning, where the weights (memristor conductance) can be changed incrementally by applied voltage pulses following desired learning rules. In addition, for applications requiring processing raw signals

from sensors and other devices, the compute can remain in the analogue domain and can thus further reduce energy, latency and chip area by eliminating the need for expensive conversion to and from digital signals.

In- memory computing

RRAM – Resistive Random Access Memory is ideal for reconfigurable, general purpose, in-memory [72] computations because of the features associated with this memory as enumerated below:

- Scaling to sub 10nm feature size
- Retention of memory state for years
- Sub nano-second switching speed
- Long write-erase endurance
- Low programming energy in the range of nano-Amperes
- Elimination of bottle necks like von Neumann and data congestion
- Low-power real time learning
- Searching large databases
- Efficiently scheduling resources or solving highly coupled sets of differential equations
- Network topology inspired by biology owing to memristors behavior

These features provide capability to build low-power highly-efficient hardware systems for different types of data-intensive tasks.

General inference leads to the fact that the memory processing unit using memristors can perform wide range of tasks like storing of data, arithmetic, logic and neuromorphic computation using the universal physical fabric, programmable to the individual device level, without moving the data outside of the fabric. Also that memristor based memory processing unit architectures may be considered as a natural progression of the computing model/pattern, following the same trend from

central processing units to graphics processing units by moving towards fine-grained and massively parallel structures.

2.7 Current Memristor Applications and Research Areas

Myon Robot

Concept – Mitigation of von Neumann bottleneck by utilizing the memristor's ability to store and process data in same physical location.

Myon [73] caters to the idea of humanoid robot. In it the individual joints performs numerous and varied actions which are excitation dependent. These actions are implemented through bio-inspired supervised artificial neural networks. Control strategies are many, like moving the limb up, down, right or left from the current position to the predicted position and maintaining the final position static unless otherwise instructed. The original approach involving traditional artificial neural networks for the controlling process is robust and stable but suffers from disadvantages like more energy consumption and inefficient limb movement.

Memristor provides new, power efficient, fast and healthy adaptation strategy for control mechanisms. It is mainly due to the unique working of memristor wherein data processing and storing is at the same physical location. Memristor also provides paradigm shift to nature of computing and using the concept to implement the working of Myon in accordance requires sound understanding of the theoretical foundations of memelements.

Benefits using memristor based computations can be reaped once it establishes demonstrated benefits over the conventional computing paradigm in terms of vital parameters like speed, percentage savings in energy consumption and adaptability of new circuits using memristors – the aim of Myon.

Cog Ex Machina & MoNETA: Modular Neural Exploring Traveling Agent

Concept – To persuade computer to act more like brains

Cog Ex Machina (Cog) [74] aims to realize machine intelligence through synchronization of hardware and software solutions. The Neuromorphic Labs at Boston University and HP Labs have joined hands and are laying the foundations for infrastructure requirements. Cog will be a new memristive computational platform that will emulate biological brain structures using flexible modeling tools developed by using converging ideas from neuroinformatics, neural modeling, material science, neuromorphic engineering, computer science and other related fields and areas. Additionally, it will allow room for using combination of conventional and neuromorphic hardware thereby creating heterogeneous processing environment to implement variety of biological-scale neuromorphic algorithms. Specification of Cog includes its design to incorporate dense memristive memories close to or on top of computing cores.

<u>MoNETA – Modular Neural Exploring Traveling Agent</u>

The objectives of the projects are as depicted

- Enhance our understanding to construct adaptive and simulated robots by creating innovations in brain modeling through advancements in software and hardware.
- Prepare adaptable framework for general purpose high performance computing platform to absorb impacts generated by innovative technology applications.
- Through complex multi threaded integration of capabilities of new hardware, demonstrate autonomous and intelligent behavior, in robots and virtual animates.

Given the objectives the MoNETA [75] project comprises of algorithms and advancements procured under Cog initiatives. Complex behaviors are successfully demonstrated by the Cog algorithms by incorporating functionalities like motivation, navigation, decision making and perception.

Computational Intelligence And Neuromorphic Computing Architecture – Artificial versus Synthetic Synapse

Concept – Explore reach of computational intelligence for neuromorphic computing to perform intelligent tasks using memristor as artificial synapse.

Human has been trying to implement intelligence artificially in to machines by developing computational intelligence and exploring neuromorphic computing options [76]. For this large high-performance computing clusters are being used thereby bringing in the challenge to limit and realize the computation to single core parallel computing processors for neuromorphic computing architects, which requires research on memristor to realize

- Analog computation based on memristor devices
- Relate physical behavior of memristor to the biological synapse

This requires proper understanding to model physical statistical variation on which electronic operation of the memristor array device depends. Also, it calls for efforts to prototype ultra large-scale memristive computing devices on a massive scale to look into possibilities to build single core large scale neuromorphic computing processor simultaneously generating information processing in a novel paradigm that will have capacity to resolve new class of problems in artificial intelligence domain having ability to infer near accurate information based on deficient or partial information to arrive at/produce accurate decision.

To achieve this it calls for elaborate planning to develop and implement device compact models, simulations of circuits, computing architectures to deploy large range applications of neuromorphic models.

Reconfigurable Memristor Fabrics for Heterogeneous Computing – CMOS/Memristor hybrid technology with 3D memristor integration

Concept – To explore unique characteristics of memristor to realize heterogeneous computing platform to supersede CMOS based architecture.

Current technological issues and challenges pertaining to CMOS are

- Controlling random manufacturing variations for scaling and integration
- Aging leading to degradation
- Failure in the early stages of the device life cycle

This causes complete collapse of system performance due to formation of non-functional memory/logic blocks. Current mitigation technique involves dynamic run time deployment of preconfigured blocks as per computation requirements.

Development of memristive based fundamentally new computing fabrics [77] is the important alternate solution to the issue mainly because the problem is vital to elaborate variety of nano-computing systems but addressable with help of current technology's capability to realize super ultra-low power very high-concentration nonvolatile memory devices. The advantages this new memristor based technology offers are:

- Switching at high-speeds ~ 1ns
- Offers Terabit density
- Data retention to more than 6 years
- CMOS compatibility to built hybrid CMOS/Memristor architectures

The properties of these fabrics enable significant breakthroughs in life impacting domains like electronic health care, simulations for natural disaster, complicated analysis of scientific data, mass storage devices, electronic business to name a few. It can be inferred that new computing fabrics thus possess the strong capability to perform heterogeneous computation activities by optimizing the system

requirement based on the available resources resulting in massive power and performance enhancements compared to traditional and long established CMOS architectures.

Statistical Memristor Model and its applications in neuromorphic computing – Synapse variation control

Concept – Address parameter fluctuations [78] in device induced due to variations in the process owing to technology shrinkage

Unique properties of memristor especially the nonlinear hysteretic curve, creates extensive opportunities in design of future systems using memristive synapse for neuromorphic circuit design but the issues arising due to shrinking of technology are

- Process variations leading to device parameter fluctuations affecting device electrical characteristics
- Worsening of the electrical response of memristive system when the analog states of memristor may change due to addition of any instantaneous memristance.

This calls for systematic evaluation of effect of process variation on the memristive behavior for which the contributing factors are

- Random uncertainties in lithography processes leading to line edge roughness
- Formation of atom mounds due to deposition process and coarsening with time leading to thickness fluctuations
- Disproportionate shrinkage of geometry variations with respect to technology

Methods to mitigate the issues can be

- To investigate variations in geometry and its impact on electrical properties and hence circuit design

- Develop algorithms to imitate variations in geometry to expedite multi-dimensional memristor structures.

2.8 Research Gaps

Based on literature survey the research gaps identified are as enumerated

- To investigate the following phase change phenomenon in materials
  Crystalline to Amorphous phase transition
  Metal to Insulator phase transition
- Investigate dependency on temperature of these phase change phenomenon
- Investigate advantages related to phase change in materials like
  Memory effect
  Mechanisms to control the memory effect
  Physical scale/dimension at which these effects become effective
  Investigate applications based on phase change phenomenon like
    - Ultra high density nonvolatile memory
    - Synapse of a brain
    - Multi level bit storage capacity
    - Power savings
    - Reliability
    - Changes necessary to conventional CAD tools

2.9 Reasons to Reach to Research Gaps

- Scaling issues as cited by Gordon Moore and Dennard
- Limitations of mitigation methods adopted by industry to stay afloat to carry forward with Moore's Law
- Limitations of conventional von Neumann and Harvard computer architecture
    - Need to process information while travelling on data bus and prior to reaching the intended peripheral or the CPU.

- Look alternate method to store information to reducing or eliminate the dependency on charge which is fundamental in conventional and popular memories like DRAM, SRAM & FLASH to store the information.
- Need to investigate models that would accommodate non-linear dynamics
- To achieve precision in non-linear dynamics conductive filament for Multi Level Bit Storage
- To address issues related to
  - Switching variability to check the variation in resistance of phase change switch
  - Reset Current Reduction to distinguish between different logic levels
  - Reliability in terms of data retention by the phase change switch/individual memory cell
  - Estimation of Memory behavior and cell array reliability with the help of different tools in analog and digital domains like SPICE and Modelsim
  - To explore FPGA based solutions to provide the simulation and synthesis opportunities at 14nm to 180 nm size

2.10 Problem Statement

Memristor is a very recent addition to the group of passive components. It has remarkable characteristics namely: inherent existence at nano-scale in many materials through multiple physical mechanisms, existence of memory effect and storing it in form of a resistive value and behavior as a synapse of a brain. Cumulatively, it leads to solutions to long pending issues like super high density nonvolatile multilevel bit information storage in resistive domain, direct solution to von Neumann and Harvard architecture bottleneck by allowing processing of information while travelling on data bus, solution to scaling issues predicted and pertaining to Moore's law, behavior as synapse of a brain. Looking into these advantages the problem statement devised is **"Simulate memristor based**

memory cell based on amorphous to crystalline and metal to insulator phase transitions and its behavior in analog and digital domains".

2.11 Objectives

- Simulate memristor based phase change memory application based on two phenomenons
  - Amorphous to crystalline phase transition
  - Metal to insulator phase transition
- Simulation of memristor based phase change memory application behavior in analog and digital domain
- To investigate temperature effect on Phase Change Memory cell
- To investigate variability, reliability of PCM arrays of different temperature

Summary

The chapter tries to summarize the literature related to memristor and memristive technology, its impact, applications and further progress. Presented are research gaps, reasons to reach top research gaps, problem statement and objectives.

CHAPTER – 3
PHASE CHANGE PHENOMENON

This chapter describes nonvolatile Phase Change Memory (PCM) Cell and Metal Insulator (M-I) phase change memory cell. It describes memory effect, characteristics and switching mechanism in phase change material. Further the different materials are reviewed for switching mechanisms and are classified in accordance. The PCM & M-I cell structure and SPICE programming concepts are detailed. The chapter includes the complete description in detail to support the cause related for devising new and reliable memory.

3.1 Phase Change Memory

Chalcogenide compounds falls into the category of phase change materials and are ideally suited for storage of information. These chalcogenide materials and their property behavior mainly, reversible amorphous and crystalline states, have reached maturity owing to thorough investigation over long time duration. This has paved path for growth of current phase change based optical/ocular as well as electronic means of storage. These materials form the foundation of the applications like:

- Re-writable compact disks – CD,
- DVDs – Digital Versatile Disk
- HD (High Definition) Blue Ray Disks
- Electronic Phase Change Material Devices

3.1.1. Historical Perspective

- **1900**, A. T. Watermann *et al*. [79] discovered very large scale negative resistive coefficient in MoS_2, a chalcogenide semiconducting material.

- **1962**, A D Pearson *et al*. [80] at Bell Laboratory mentioned steady and reversible transition between two conducting states/regions achievable by controlled application of electrical pulses in the material As-Te-I glass.
- **1968**, Stanford Ovshinsky *et al*. [81] contributed immensely by developing electrically controlled threshold switching device and memory switching device respectively. He is known as father of phase change memory.
- **1970**, G E Moore *et al*., [82] demonstrated 256 – bit (16 × 16) phase change material based memory array consisting of a *p-n* junction diode with a memory storage element.
- **1974**, Feinleib *et al*. [83] laser induction based optical memory process in chalcogenide materials leading to modern day applications like CD – Compact Disk and Digital Versatile Disks.
- **1978**, R R Shanks *et al*. [84] demonstrated 1024-bit Phase Change Material Memory array.

Extreme high-power consumption prevented commercialization of phase change material based device applications mainly because of direct proportionality between required energy to switch phase of material with quantity of active phase change material. The need to reduce the feature size from 10 µm to 180 nm in 1990s brought the advancements in the lithography technology leveraging an opportunity to address the issues related to high programming power necessary to program phase change material based devices.

The results emboldened the future strategy for development of the PCM devices.

- **1990**, Panasonic introduced rewritable CD based on the principle of optical phase change storage.
- **1999**, Tyler and Parkinson commercialized Phase Change Memory through the joint venture called Ovonyx

- **2006**, BAE commercialized PCM devices for space applications based on their property of being hard to radiation. It was a 512KB × 8 array for 4MB memory device operating at 3.3V and fabricated using 0.25μm bulk CMOS process.
- Currently, the aim of companies like NXP, STMicroelectronics, Numonyx (now Micron), Hitachi, IBM, Samsung Electronics, etc is to find techniques for full scale development and commercialization of phase change material based products like stand alone super ultra high density nonvolatile memories as storage class memory.

The recent developments lead to healthy proposals for application of phase change material devices in super high density nonvolatile memory systems constituting to robust application drive/thrust for the emergent technology. Essential desirable characteristics for PCM devices for memory application are low power consumption, long data preservation, high endurance and scalability. Simultaneously, the challenges exist in the form of impact of crystallization kinetics, erase and write speeds, and examination of the deterministic or stochastic processes associated with the operation of phase change material devices which calls for systematic investigations. A useful beginning area to customize the phase change technology for application as memory can be ongoing research related to multi bit programming and control of kinetic mechanism related to crystallization of chalcogenide material.

Computing capacity determines the ability/performance of the electronic devices. However, access time of the memory and power expenditure in memory subsystem provides limitations on this computing capacity. Measures like scalability of SRAM, realization of implanted/embedded DRAM in memory subsystem (which is a self contained system of a larger system), in addition to Flash memory as substitute of Hard Disk Drives (HDD) has subjected conventional memory technology to stress. These developments indicate towards the need and potential of ultra high density nonvolatile memory as an embedded technology. Research

points to serious competition to conventional memory technology from super ultra high density nonvolatile memory technology like those conceptualized on the principle of reversible change of phase of materials. Read, write, retention, endurance capacity, cyclability, and addressability of these new memory devices reach up to individual elements and methodology used is different from the conventional ones. The features of new memories include immense improvements in power consumption and speed provides opportunity to completely rethink the memory subsystem's design. The technology suggests changes in memory technology from fundamental aspects with potential to performance of the devices positively and will reflect in form of devices with immense increase in computing capacity with very low power consumption.

3.1.2 Memory Effect and Characteristics of PCM Material

V-I characteristics based behavior of PCM material is depicted in Fig. 3.1 in which resistance decreases and current increases as the application voltage nears/reaches to threshold voltage V_{th}.

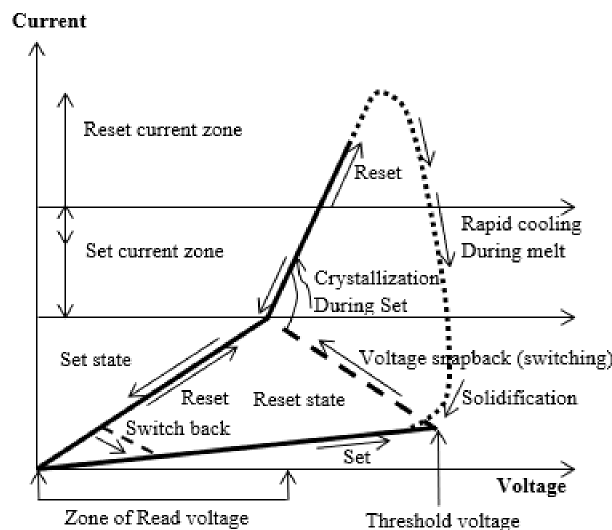


Fig. 3.1 *V-I* Characteristics of threshold switching

The process is equivalent to switching of resistance to high value at low voltage. This voltage snapback at V_{th} is called switching. Flow of large current through the material causes Joule heating of the material and simultaneously changes the phase of material from amorphous to crystalline [85]. Crystalline phase is attained at low temperatures. The phase change of the material results into memory effects. PCM materials are designed to switch between two phases.

Maintaining the state of the material after switching is an important criterion because it retains the memory effect in form of a state in the material. Multistate operation is feasible because the material switching may take place to any one of the crystallized state, mainly because the material may attain different degrees of crystallization, hence many resultant crystallized states. Chalcogenides materials (Ge-Te, $GeSeTe_2$, $Ge_2Sb_2Te_5$, $AgSbSe_2$, Sb-Se, Ag-In-Sb-Te, to name a few) are candidate material for phase change material based memory applications owing to element divalency and non-bending and bending flexibilities of single electron pair. Mechanism involving this kind of disordered materials revolves around or based local atomic number. The desired property i.e., the change of phase is formed either by irradiation of light or by use of a pulse of voltage.

3.1.3 Switching Mechanism in PCM Material

Viscosity enhances when the melted phase change material undergoes the cooling process thereby reaching a point wherein the material structure stops following the temperature change as shown in Fig. 3.2. The combination of this property with cooling speed ends up in either crystalline (Set/low-resistance) or amorphous (Reset/high-resistance) state. If cooling speed is low the material has the liberty to reach to equilibrium crystalline phase and conversely to amorphous phase, by the process of quenching resulting in the material achieving a disordered phase frozen to glass. The property of interest is the large resistance contrast between the two phases which is primarily utilized by phase change based devices [86]. The contrast in resistance is up to the order of 3 to 4. The phase transfer, to reach to either of one

state i.e., amorphous or crystalline, is produced by the process of annealing by changing the temperature of phase change material between melting and glass transition temperatures.

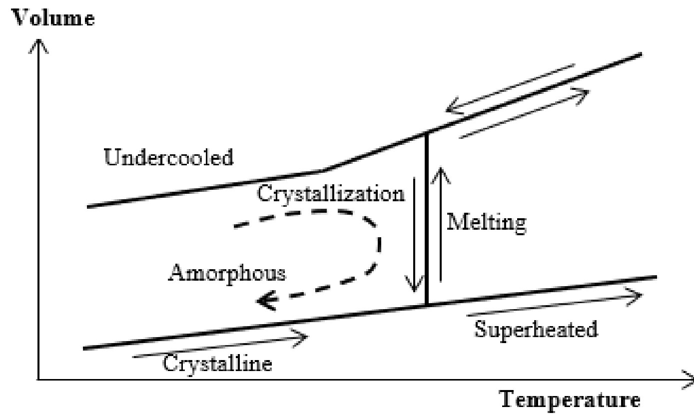


Fig. 3.2 Formation of amorphous and crystalline phases

The general procedure of annealing involves applying a laser or a current pulse with varying degrees of intensities and durations depending on the state to be achieved.

3.1.4 Classification of Physical Mechanisms Depicting Memristive Effects

Based on different mechanisms the memristive effects are broadly classified as follows and are tabulated in Table 3.1 to Table 3.4 respectively.

- Memristance [87]
- Memcapacitance [88]
- Meminductance [89]
- Other systems with memory

Table 3.1 Classification scheme of memristance mechanism

Effect – Memristance
Mechanism – Resistive change
• Thermal effect • Chemical reactions

• Ionic transfers • Spin polarization • Phase transition

Table 3.2 Classification scheme for memcapacitance mechanism

<table>
<tr><td colspan="4">Effect - Memcapacitance</td></tr>
<tr><td colspan="4">Mechanism – Geometrical and Permittivity related</td></tr>
<tr><td>Geometrical</td><td colspan="3">Permittivity related</td></tr>
<tr><td rowspan="2">• Elastic
• Redox reaction
• Charging</td><td>Delayed response</td><td>Spontaneously polarized medium</td><td>Permittivity switching</td></tr>
<tr><td>• Tunneling
• Ionic Transfer</td><td>• Ferroelectricity</td><td>• Ionic doping
• Phase transition</td></tr>
</table>

Table 3.3 Classification scheme for meminductance mechanism

<table>
<tr><td colspan="4">Effect – Meminductance</td></tr>
<tr><td colspan="4">Mechanism – Geometrical and Permeability</td></tr>
<tr><td>Geometrical</td><td colspan="3">Permeability related</td></tr>
<tr><td>• Thermal
• Elastic</td><td>• Permeability switching</td><td>Spontaneously magnetized medium
• Ferromagnetism</td><td>Delayed response</td></tr>
</table>

Table 3.4 Classification scheme for other systems with memory

<table>
<tr><td colspan="2">Other systems with memory</td></tr>
<tr><td>Three terminal devices</td><td rowspan="2">Memristive component in Josephson junction</td></tr>
<tr><td>• Electrochemical cell
• Solid state memrister
• Ploymeric transistor</td></tr>
</table>

3.2 Physical Mechanism and Memristive Phenomenon in Various Materials

Gradual hysteretic switching characteristic is observed in most materials. It indicates dynamic nature of the material at atomic level, thereby making the material to evolve through different values i.e., the state. The material freezes in the current state when the external stimulus is removed and this permanent state is called memory effect. Upon varying the stimulus the value of memory state changes. This important property allows multi bit memory storage in single memory cell thereby opening the avenues for very high density memory technology [50 to 38]. The materials in Table 3.5 displays robust characteristics in favor of super very high density nonvolatile memory and its applications which includes high-speed read and write times, large ON/OFF ratios, possibility to fabricate small size cells and suitable range of programming voltages.

Table 3.5 Classification of physical mechanisms in different materials

Memristive phenomenon	Material	Physical mechanism
Phase change [90]	Ge-Te, $GeSeTe_2$, $Ge_2Sb_2Te_5$, $AgSbSe_2$, Sb-Se, Ag-In-Sb-Te	• Electrically induced switching amid amorphous/formless and crystalline states due to Joule heating, because of flow of current, identification of cell status by probing its resistance value. • Exclusion/removal of oxygen atoms resulting in collapse of local energy gaps, also causing rearrangement of localized atomic structure • Ionic transport • Electrochemical reduction (solid-state redox reaction)
Binary oxides [91]	TiO_2, CuO, NiO, CoO, Fe_2O_3, MoO, VO2	
Nanogap systems [92]	SiO_2, NiO	
Perovskite-type oxides [93]	Pr_{1-x}-Ca_xMnO_3, $SrTiO_3$:Cr	
Sulphides [94]	Cu_2S, Ag_2S	
Semiconductors [94]	Si, GaAs, ZnSe-Ge	

Organics [95]		• Complex interplay between spin degree, lattice and charge • Spin degree freedom • Hodgkin Huxley – ionic transport

3.3 Properties of Different Materials for Memristor

Table 3.6 elaborates various properties of different materials like noise margin, either voltage or current driven, size of device, scaling factor, On-Off ratios, switching speeds, thermal stability, phase change property, ionic transport, resistive filamentary properties, applications areas of memristors.

Table 3.6 Memristive properties in various materials

Material	Properties
TiO_2	Enhanced memristive performance with less noise, peak current of .04Amp at 5 Volt implying more conductive nature
SiO_2	Resistive switching in metal free embodiment , switching through voltage-driven formation and modification of silicon nano-crystals, small size ~5nm i.e., scaling to ultra-small domains, healthy nonvolatile property, high OFF/ON ratios > 10^5, enhanced switching speed to sub–100nm, robust endurance with 10^4 read erase cycles, CMOS compatibility for constructing logic devices and memory devices
HCuPc	Fabricated thermally stable nanocomposite having high electric field and high temperature dielectric applications
SAM	SAM – Self assembled monolayer is a nonconventional technique to avoid high production cost and long processing time. Easy controlled adjustment of key parameters in molecular and organic electronic devices. SAM suggests unipolar or bipolar switching, low to high resistance current ratio between 10 to 100, ON/OFF ratio of 100, fabricated ReRAM device density of $1 \times 10^{10}/cm^2$

Fe_2O_3	Gradual change in resistance (memristive) and capacitance (memcapacitance) with repeating voltage polarity at the same time owing to nanoparticle assembly. Memristive and capacitive characteristics resembling (biological) synaptic depression and potential motions indicative of potential applications in neuromorphic hardware and analog nonvolatile memory and circuits
NiO	Key phenomenon is resistive switching in ReRAM due to binary transition metal oxide (TMO) cells. Phenomenon is rupture and formation of conductive filaments. The conductive filaments comprise of oxygen vacancies or cation interstitials which results in change of microscopic oxygen stoichiometry. Cell size is $4\times4\mu m^2$, $20\times20\mu m^2$ and $88\times88\mu m^2$ single &two forming and non-forming respectively
PEDOT: SS	A conductive metal filament is formed in the centre of the layer of organic material in Ag/ply(3,4-thylenedioxythiopene): poly(styrenesulphonate) (PEDOT:PSS)/Pt component. A bipolar filamentary resistive switching state results that falls in the category of electrochemical metallization. Potential applications are in the area of artificial synapses since change in filament has close association to synaptic plasticity appearing in LTP, STP, LTD, and STD
VO2	VO2 is a material of choice owing to quick response time, enhanced range of attainable/accessible resistive values via metal to insulator (MIT) transition. Resistance change is four orders of magnitude
GO	GO – graphene oxide is a good semiconducting/insulating material suitable for ReRAM. Automatically thin 2D of GO allows scaling above the current limits specified for semiconductor technology and high-density fabrication is possible. GO based resistive memory has many benefits like cost effective device fabrication, easy synthesis, compatibility for flexible device applications and scaling down to few nm. Properties also include thermally stable, forming free, multibit storage, flexible and high OFF/ON resistive ratios at low voltages

PZT	PZT is lead zirconate titanate, a piezoelectric material, considered for memristive applications. Use of this material is possible because heterogeneous integration of technologies by integration of material physicists, computational chemists and bioengineering to explore nonvolatile memory application area

3.4. PCM Cell Structure, SET/RESET Operation and V-I Characteristics

The memory cell construct/organization based on phase change concept is depicted in Fig. 3.3 (a), wherein, the programmable phase change material, to which the heat is supplied by means of a heater, is placed/sandwiched in amid the top and bottom electrodes [96]. A high resistance (Amorphous/Reset state) of PCM cell is attained by the application of a small period high magnitude electric pulse.

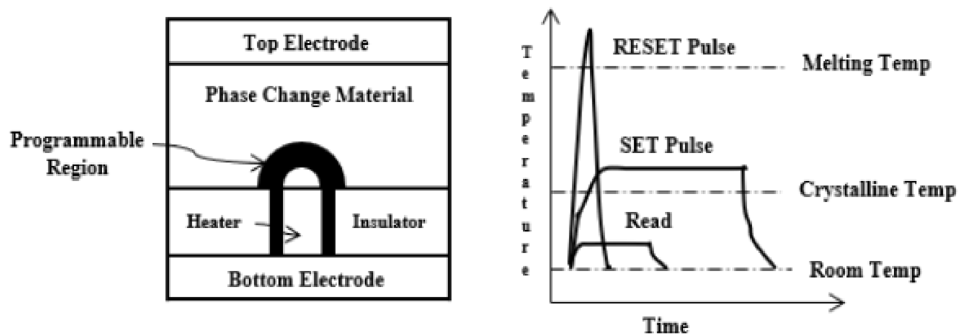


Fig. 3.3 (a) PCM cell structure (b) Read operation of PCM cell

Owing to this material melts, and upon removing the pulse abruptly, molten material quenches and heads for high resistance (Amorphous/Reset) phase. This region generally is in series/progression with crystalline region and ultimately determines the effective resistance of the memory cell between bottom and top electrode contacts.

To achieve the low resistance set phase, a considerable portion of the PCM cell is heated above the temperature needed to crystallize the cell. This is achieved via application of a current pulse of low intensity for relatively long duration. The PCM cell is read by passing a tiny value of current all the way through it. The value of

read current is small enough to not disturb the status of the cell as is shown in Fig. 3.3(b).

3.5 Need for Simulation

Promising research ideas are converted into products by the industry. Depending on the projection of the product by the industry followed by mass appeal and usage its longevity and hence profits are decided. Many industries opt for established products but few adopt risky divergence and foray into new fields where technology knowhow is less. This shift in an unfamiliar field may prove to be an expensive liability, since transition in itself calls for new infrastructure establishments asking for costly investments over significant time durations.

First product is a challenge from many aspects and necessitates huge research and development inputs without the guarantee of success of its first product. Even if successful then mass production remains a big issue. This spoils the likelihood of succession to next generation products that may possibly have been contemplated at early stages, thus forcing untimely exit with realization to initiate the learning process on the whole. This necessitates recognition and understanding of critical hurdles and device methods to bring in acceptable answers, simultaneously keeping an eye on the distant prospect of technology projection. Indispensable parameters involve complete and suitably correct and thoughtful perceptive about fundamental physics and detection of set of decisive device specific characteristics. Owing to such conditions, the job of reasonably priced simulation tools and technology becomes very much important for the reason that it assists in forecasting close to predicted development of the product and the rationale validating the tool's generous utilization [97]. Also, it can practically be utilized unlimited times to validate the outcome. It provides prospects to devise and study intricate circuits, examine varied areas and to arrive at to the preferred application. However, dependable and appropriate method for precise modeling is the necessity.

Out of many, SPICE is also one such software simulation technology which is utilized comprehensively for many decades now. It makes available numerous features akin to dependability, flexibility, accuracy and, but calls for early precautions pertaining to several limitations and specific features of SPICE, to avoid situations in which the solution reached may be burdened with errors. In case of simulation of memelements, imperfection arises because classical algorithms prove ineffective leading to corrupted solutions via accumulation of numerical errors during analysis. Behavioral analysis of memelement models, deliberately kept free, from inherent parasitic effects is an ideal model. These are simple from computation view point but important to understand the fundamental properties. However, it raises a question on the precision, reliability and accuracy of the model from practical usage viewpoint.

Generally, the models pertaining to memelements are created by being keen on accurateness of the study and deviation and concurrence issues are recognized by infringement of distinctive characteristic fingerprint of the memelement. They are customized by means of set of laws of behavioral modeling, suitable setting of options and parameters of program. Objective is to prevent convergence problems while analyzing the circuits and to solve them in shortest time span, thereby calling or a compromise between reliability, speed and accuracy of the result.

The base of modeling is the differential equations of the memelement. These equations are liable for variables related to internal state, efficient control of parameters of the port to memcapacitance, memristance and meminductance, ensuing into element ports of memcapacitive, memristive and meminductive environment correspondingly. This results to splitting up of memelement model to two or more sub-models. A mixture of behavioral and conventional modeling is used in SPICE program setting to produce the desirable circuit behavior as an output. Generally, the equations defining the state of the process are modeled as an

integrator circuit consisting of shunt 1F capacitor with a governed current source. A grounded, very high value resistor provides DC path.

The circuit is built for the following:

- Equivalence between quantity being integrated and current supply is maintained
- Computed integral for the duration of the analysis is produced by shunt capacitor

The memristive, memcapacitive and meminductive ports are modelled in accordance. Memelements namely; memristor, mem-inductor, and mem-capacitor can be well thought out to be the electronic devices: resistor, inductor and capacitor having the capacity to remember. Their innate feature is to keep hold of information when no power is available. The mathematical depiction of memelement is as enumerated,

$$y(t) = g(x, u, t)\ u(t) \quad (3.1)$$

$$\dot{x} = f(x, u, t) \quad (3.2)$$

Here

u(t) & y(t)	=	Circuit variable; the current, voltage, flux and charge *u(t) & y(t)* represents input and output as well,
g	=	Global answer
x	=	*n*-dimensional vector (of internal state variables)
f	=	Continuous *n*-dimensional vector function.

Example case of ideal memristor model for SPICE simulation

The charge dependent memristance R is defined as follows

$$V_M = R\left(q(t)\right) I \quad (3.3)$$

Here charge and current are related through time derivative

$$I = dq/dt \quad (3.4)$$

However, equations eq.(3.3) and eq. (3.4) are not directly used and more common model is based on paper [13] wherein entire memristance is summation of resistances of two regions and is mathematically represented as

$$R(x) = Ron(x) + Roff\ (1 - x) \qquad (3.5)$$

Here, R_{on} and R_{off} are limiting values of the resistances and x Є |0, 1| defines the location of the boundary. The equation of movement of x is written with a window function as

$$\frac{dx}{dt} = k\ W(x)\ I \qquad (3.6)$$

Here k is a constant and its value lies between 0 to 1 [102].

And $W(x) = 1 - (2x - 1)^{2p}$ (3.7)

Where p is a positive integer [102], varies between 1 to 100.

Window functions models the working of the memristor by preserves the internal state variables. Internal state variables defines the working of the memristor by describing physical processes that takes place inside the memristor. They are specified by k and p in Eq. (3.6) and (3.7) respectively.

However, Eq. (3.6) can be represented as

$$\int \frac{dx}{W(x)} = k\ I \int dt \qquad (3.8)$$

$$\int \frac{dx}{1 - (2x - 1)^{2p}} = k\ q(t) + q_o \qquad (3.9)$$

Since

$$W(x) = 1 - (2x - 1)$$

$$\int \frac{dx}{1 - (2x - 1)^{2}} = k\ q(t) + q_0 \qquad (3.10)$$

For p = 1

$$\int \frac{dx}{1-(4x^2+1-4x)} = kq(t) + q_0 \qquad (3.11)$$

$$\int \frac{dx}{4x - 4x^2} = kq(t) + q_0 \qquad (3.12)$$

$$\frac{1}{4}\left[\int \frac{dx}{x} + \int \llbracket \frac{dx}{(1-x)}\right] = kq(t) + q_0 \qquad (3.13)\rrbracket$$

$$\frac{1}{4}\log\frac{x}{1-x} = kq(t) + q_0 \qquad (3.14)$$

Here, q_0 is an integer constant or initial condition

Hence memristance can be represented as

$$R\big(q(t)\big) = R_{off} + \frac{R_{on} - R_{off}}{e^{-4k(q(t))+q_0)} + 1} \qquad (3.15)$$

Considering initial memristance Rini = R(q=0), eq. (3.15) becomes

$$R\big(q(t)\big) = R_{off} + \frac{R_{on} - R_{off}}{ae^{-4kq(t)} + 1} \qquad (3.16)$$

Where

$$a = \frac{R_{ini} - R_{on}}{R_{off - R_{ini}}} \qquad (3.17)$$

Eq. (3.15) assists in modeling a reliable model in SPICE environment, wherein the state variable is the charge ‘q’, which can be obtained by integration of the current source by the capacitor. This allows reciprocity between charge and node voltage. The SPICE circuit is depicted in the Fig. 3.4 below and consists of a fixed R_{off} resistor and a controlled voltage source. Emphasis is on the fact that accurate model is possible when supported by pertinent physical phenomenon.

The top-down design approach is based on the behavior model of the system design. In top-down approach the behavioral model is distributed into small fragments called modules. The breaking process of the system into smaller modules optimize the complications occurred during the designing of the model. On the other hand, in bottoms-up approach, the model is designed from base level, each module is designed independently and structured together to complete the process in structural style of modeling.

In the design of the SPICE model pertaining this thesis, the top-down approach is followed since it requires less response time/delay in comparison to the bottom-up approach. The structural base model takes more memory space and delay in the hardware chip design in comparison to top-down approach.

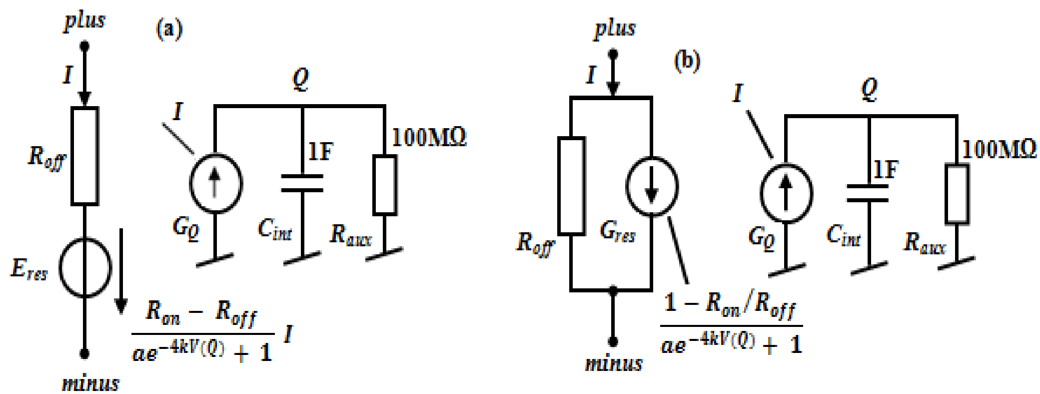


Fig. 3.4 SPICE model of ideal memristor

Summary

The chapter summarizes the phase change phenomenon and tries to exemplifying that it is diverse in nature and existent in wide range of materials. The phenomenon has multifaceted capacity to directly address the bottlenecks being faced by semiconductor industry and simultaneously possesses the capacity to device applications in analogous mode in areas like neuromorphic hardware, artificial intelligence, ultra high density nonvolatile memory, robotics to name a few. Memristor and its applications promise next generation industry revolution.

CHAPTER – 4
METHODOLOGY AND TOOLS

The chapter describes the design methodology and methods used for the material study, PCM application in analog and digital domain. The chapter describes the software tools from simulation and synthesis aspects. It also details the complete environment of functional simulation and logic verification.

4.1 Methodology

Methodology revolves around identification of the range of physical phenomenon responsible for different memristive behaviors in various materials. Most important aspect is to determine whether the memristive *V-I* curve follows, fits and resembles the characteristic fingerprint i.e., zero crossing hysteretic curve followed by distinguishing the parameters responsible and fitting the physical changes into mathematical equations case by case.

In case of phase change memory cell, the reversible memristive physical phenomenon is changing phase of the material between amorphous to crystalline which satisfies the characteristics finger print prescribed for the memristive behavior. The parameters responsible are temperature, crystalline factor, etc. The physical changes responsible are formalized into mathematical equations and simulation software/tools use these equations to generate models popularly known as behavioral models. These models are further used to design circuits and utilities as per the need which here is ultra high density resistive nonvolatile memory.

Ngspice simulation tool is used for designing and analyzing the analog behavioral model of the phase change cell followed by Xilinx and Modelsim simulation tools to analyze the multi level memory storage capacity, reliability and endurance.

Design Constriants

- Select the GST for PCM and M-I phase transition material for the memristor for phase change memory applications

Design Apporach

- Select the design appoach of single cell PCM and for memory arrays of different sizes as the botton up approach or the top to down apporach

Modeling Apporach

- The design is following the VHDL based modeling and design. It has the data flow, behavioral and structural models in Xilinx ISE 14.7.

Architecure Modeling

- Follow the interlinked and memory architecure with all its sub modules design and functional components. The behavioural model relaization is followed in the design.

RTL Analysis

- The PCM and PCM array behaviour model chip is having the clock signal, reset, input data, output data and address for wordline and bit line

Internal Logic Schematic

- Get the inetrnal logic schematics of PCM and PCM array behaviour model configuration that will have interlink and memory modules against each array

Functional Simulation

- The Modelsim waveform simuator is used for the functional simulation for test different test cases and inputs for all the designed chip.

Test Cases Analysis

- The different test samples and cases are used to check the output in the waveforms with different time delay

FPGA Synthesis

- The FPGA synthesis apporach is related to lock the FPGA pins in the Virtex-5 FPGA Kit, followed by logic placement, routing and burn the program in FPGA.

Parameters Analysis

- The FPGA hardware parameters are analysed for PCM (2×2), (4×4), (64×64) and (256×256) size arrays such as slices, LUTs, IoBs, and memory. The timing parameters are analysed for delay and frequency.

Comparative Analysis

- Analyze the system performance against set and reset behavior using iterative progarmming model, perform the comparision of hardware and timing parameters to estimate the performance of desinged chip with existing work in terms of hardware, memory and timing simulation.

4.2 Methodology for Chip Synthesis

The block diagram of Chip design, simulation and synthesis is shown in Fig. 4.1. The steps of the process are discussed.

- **Design Specification**: There are two approaches in PCM system chip design one is bottom up design another is top-down approach. In the bottom up technique the design is developed for small modules and structured in a top design using structural style of modeling. In top-bottom up approach the full system is considered and designed in a way that it will meet the behavior of the system. In the PCM chip design, it is essential to define the cluster size and duty cycle of the clock input signal. The designer based on company project requirement decides the design specifications.

- **HDL Modeling:** The chip design is done using any of the HDL language. The industry favorite languages are Verilog HDL and VHDL. VHDL based design is used for the problem statement of our research because the PCM design can be modeled in dataflow modeling, behavior modeling or structured modeling using VHDL. In the VHDL Code, the designer can choose any one the style of modeling for the chip design.

  Data flow model – based on the logical expression output

  Behavioral model – based on system functionality and truth table

  Structural model – based on the architecture level design modules instances and interface

- **RTL View:** RTL is directly extracted from Xilinx Software and it is the graphical representation of the design (.ngr) is the file generated with the help of Xilinx Synthesis Technology (XST) where all the inputs and outputs of the top level module is observed. RTL view is the early stage of a synthesis process before the place and route process. The internal architecture of the processes

and its behavior is checked. The design is represented in terms of multiplexers, adders, flip-flops, registers and so on.

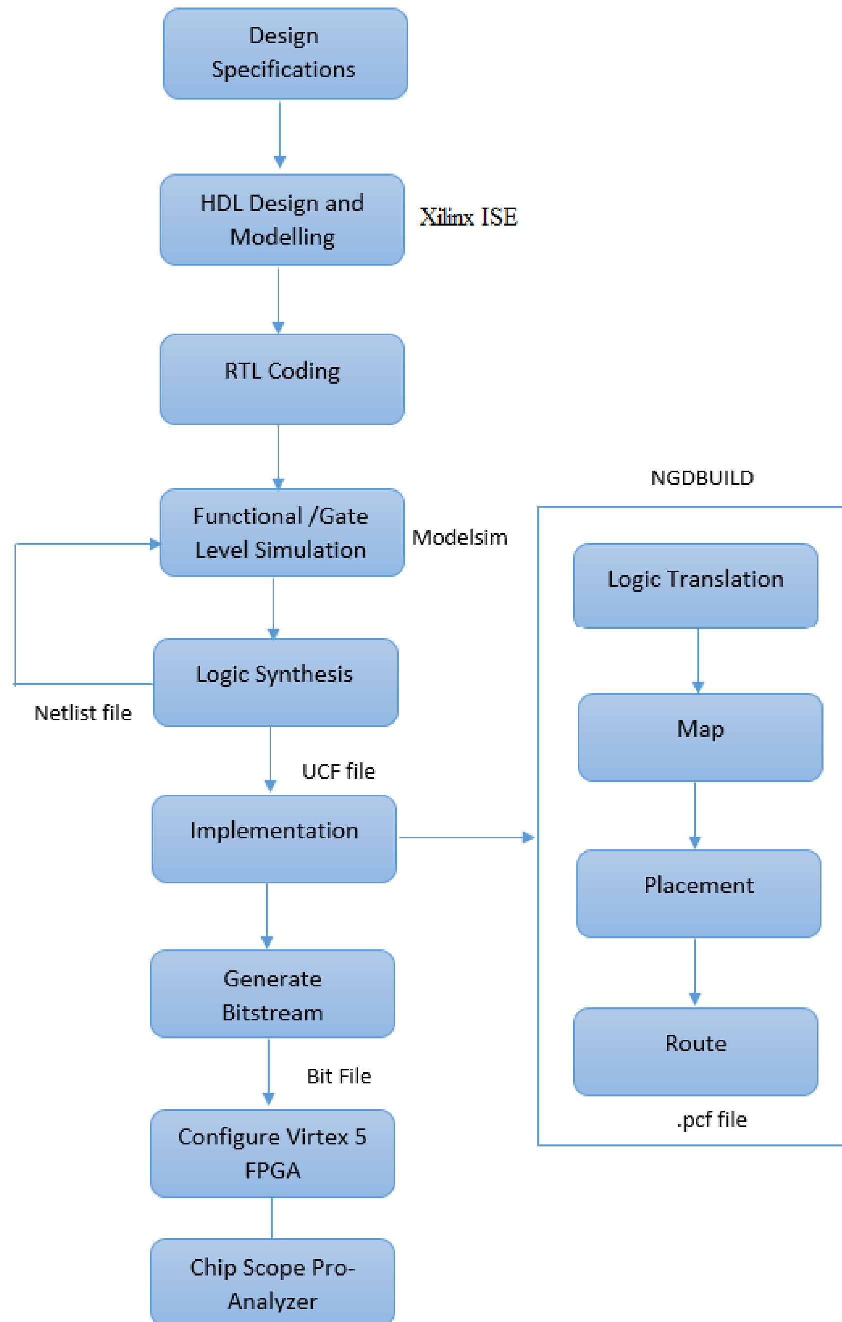


Fig.4.1 PCM System Design and Synthesis Methodology

- **Functional Simulation:** The functional simulation depends on reset circuitry, clock input and test cases. The designed chips and modules are checked by RTL view, internal schematic diagram and test cases. The designer based on the functionality of the designed chip decides test cases. RTL simulation or behavioral simulation is the timing simulation of the design, depends on the design hierarchy. The simulation is required for all the intermediate modules to under the behavior of chip for different test inputs before the synthesis to check the output waveform. In case of unsatisfied results, the designer has to go for redesign. VHDL or Verilog HDL is used in the behavioral simulation during the simulation level variables, signals are observed functions and procedures are traced and the breakpoints are set to check a sub module from the top-level module.

- **Logic Synthesis:** In the pre-synthesis, the PCM deigned chip performance is analyzed based on the hardware and timing parameters. The hardware parameters are slices, flip-flops, LUTs and memory requirements in the chip. The timing parameters are relating to combination delay, minimum time and maximum time of clock etc. If the memory utilization of the designed chip is consuming more that 100% of FPGA resources then it calls for redesigning.

- **Implementation:** Based on the view synthesis report as the hardware and device utilization summary the designed modules are synthesized on FPGA. The FPGA is interfaced with the computer in which the code was developed for specific module. The test inputs are given using switches of the board and verified using LED, LCD or monitor using VGA. FPGA has the feature of inbuilt ADC and DAC conversion. So, FPGA synthesis and experimentation is required to test the designed chip in real time application. In the module, design experimentation is done on Virtex -5, high speed FPGA. The FPGA implementation process includes the logic translation and optimization on

FPGA. The pre-synthesized code is required to burn in the core of FPGA that includes the process of technology mapping, placement and routing.

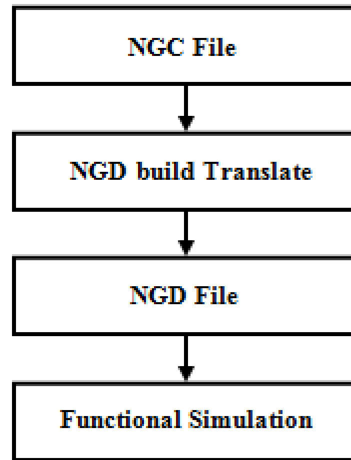


Fig. 4.2 FPGA translate

The User Constraints File (UCF) is created to configure the pins in Virtex 5, FPGA, then implementation is carried out. The implementation includes the technology mapping, placement and routing. The mapping reduces the blocks to minimize the area and logic block are placed to provide optimal wire connection between cells called routing. NGDBuild ignores any invalid location constraints (LoC) information that would result in errors. Fig. 4.2 and Fig. 4.3 shows the logic translation and mapping in NGDBuild environment.

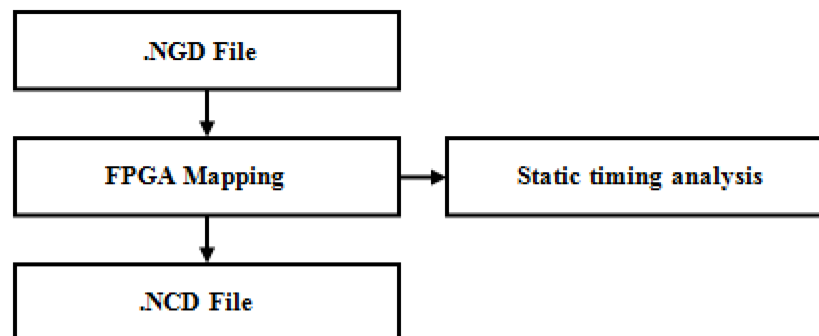


Fig. 4.3 FPGA Map

- **Static Timing Analysis (STA):** STA is the step after the mapping or placement and route processes. After mapping the timing analysis of the report list the delays in signal path of the design that derives from the logical design. After the PAR the timing information that incorporates the timing delays information which provides the detailed timing summary of the design. The analysis is very much helpful to estimate the timing parameters of FPGA such as minimum period, minimum time before clk signal, maximum timer after clk signal and total path delay.

- **Bit File Generation:** The design of the routed NCD file should be loaded into the FPGA hardware for this purpose the design should be converted into the format that is acceptable by FPGA. The FPGA burns the bit file in its core. The routed NCD file converts the bit stream file (.BIT file) to configure the targeted device in FPGA. The communication between the computer and FPGA can be done using the JTAG cable or USB cable. These steps are followed after programming in the Xilinx ISE.

- **Configure Virtex-5 FPGA:** In the process the code is configured to selected device in Virtex 5pro. In the design, XC5VLX110T is considered for the same purpose. The selected device should be matched with the device chosen during simulation and pre synthesis process in Xilinx ISE.

4.3 Software Tools

The analog domain simulations are carried out using the software Ngspice and the software used in the design of PCM chip implementation Xilinx ISE 14.7 and Modelsim 10.1.

4.3.1 Ngspice

Primarily necessary is the reliable prediction of the behavior of the circuit with the help of simulation software, which assists in reduction of nitty-gritty related to

designing and realizing of physical circuitry. SPICE ("Simulation Program with Integrated Circuit Emphasis") provides much needed solution in analog domain for issues related to designing of the circuit. It is basically a wide-ranging, open-source analog simulator.

Bread boarding discrete components is one of the popular methods to verify the functionality of a circuit. However, to bread board integrated circuits prior to its manufacturing is not a practical approach because many properties of the circuit like parasitic capacitance and resistance may vary away in terms of value upon comparison with actual printed circuit or wiring boards. Also, there are many manufacturing prerequisites related to circuit designing and these processes involves high costs, but are important to bring the working near to perfect. All this needs to look into prior to actually manufacturing the intended circuit.

Viable way out is circuit simulation procedure at individual transistor level prior to committing to manufacture an integrated circuit. Other advantages are:

- Accurate estimation of parasitic components and its effect on circuit performance
- Virtually, infinite opportunities for simulation in case the circuit designer may wish to seek additional information
- Options to include parameters responsible for deviation of the circuit performance like tolerances of components while manufacturing

SPICE simulation programs acquire a net list that describes the elements of the circuit as well as their connections to translate this description in to equations essential to study. In general the produced equations are nonlinear differential algebraic equations and require implicit integration methods, Newton’s method and sparse matrix technique to get solved.

Also, SPICE is robust and fast and provides the analysis related to DC, DC transfer curve, noise, transfer function, transient and includes range of device models. Also included is options for schematic capture and plotting, setting of initial conditions to derive transient analysis in case of circuits deficient of stable initial operating point solutions.

4.3.2 Xilinx ISE 14.7

Xilinx is one of the leading companies in the field FPGA design. It is the biggest semiconductor company to cover the front-end solutions in the chip design, verification and synthesis. In the Xilinx software, the programmers are developing the chip using latest HDL languages such as Verilog HDL, VHDL, and ABEL, etc. After the design, there are the options to see the RTL, inter schematic view and view synthesis report. The developed chip is configured using input pins, output pins and input/output pins. Xilinx has the ISIM simulator to see the waveform using inbuilt waveform simulator, which provides the functional check of the developed chip. It also has the Chipscope for FPGA signal analysis, Static timing analysis feature, verification and logical synthesis environment. Different test benches and test cases are simulated in the software environment and FPGA guarantees the chip for mask production in the market. The tool provides the exhaustive information of logic design, synthesis, simulation, verification and timing analysis. The hardware and parameters for pre-synthesis are obtained directly from the tool which also details the hardware parameters usage, memory requirements and timing values required in the design of chip.

4.3.3 Modelsim Software Version 10.1

Modelsim Software is the software given by the Mentor Graphics Company. It is a multi-language HDL simulation software works on Verilog HDL, VHDL and System ‘C’. It has the inbuilt ‘C’ debugger. It is preferred one of the best fool for GUI and Xilinx software interface. The chip design, functional simulation and

timing analysis are done using the software. It also can be integrated with MATLAB or Simulink environment with following advantages.

Benefits of Modelsim EE

- Modelsim software gives low cost chip design solution using HDL.
- Providing interactive debug using Intuitive GUI in effective time.
- It simplifies the research data and manages the project management integrated in software and hardware.
- It has outstanding technical support to give the solutions in HDL and easy to use.
- Easy to use with outstanding technical support.
- Popular ASIC libraries are available and sign-off support for all defined libraries.
- The complete platform for hardware and software debugging.
- Simplifies the functional simulation and gives testing environment for all the possible test cases, can be used to check the functionality of the designed chip.

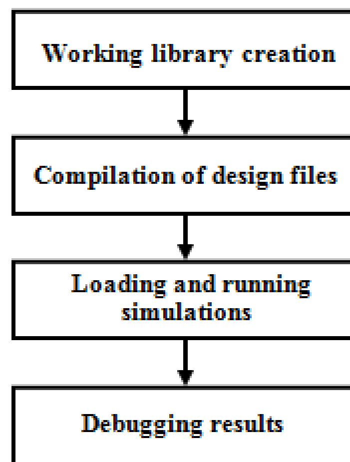


Fig. 4.4 Modelsim design process

The chip design flow and simulation block diagram using Modelsim software is shown in Fig. 4.4.

- **Creation of working library:** All the chip design based solutions in Modelsim software require the creation of the library. There is the default library in the Modelsim by the name ‘work’ which includes all the logical values and possible library functions required to do simulation by the compiler in the working library. By default the destination of all the chip design is the library in Modelsim software.

- **Designed file compilation:** The designed which is developed using any HDL, and stored in the working library is complied. The binary created by the user is suited to work on all the platforms. The designed file may be one file or grouped as the top design having submodules or structured in bottom to top level.

- **Running and loading Simulation:** The designer is loading the top module of the developed chip into the simulator after completing the compilation of the design. The loading involves the entity of chip and architecture. The design can be done in dataflow, behavior and structural modeling. The modeling of the design is chosen by the designer. Some design structured using structure style of modeling, gives better results. The design is developed in different modeling can give different timing and performance results. In the running process, it is considered that the simulation period is zero and run operations are entered by the designer to perform the functional simulation

- **Results debugging:** The developed chip may contain some errors. So, debugging environment is required to track the errors in program window. The errors are listed by the Modelsim software with respect to line and code debugging environment, help the program to check the code and take correction action in design. There are redefined scripts can be used in the software to follow the short methods. The verified results are seen in the form of waveform and timing diagrams.

Summary

This chapter detailed about the design methodology PCM chip simulation, synthesis and description of different software tools. There are two approaches in PCM system chip design one is bottom up design another is top-down approach. In the bottom up technique, the design is developed for small modules and structured in a top design using structural style of modeling. The FPGA synthesis flow has Initial design entry in VHDL, behavioral simulation, Technology mapping, placement, routing and bit file generation and configuration in Virtex-5 FPGA.

CHAPTER – 5
ANALOG SIMULATION

The chapter explains the SPICE simulation of Phase Change and Metal-Insulator transition memory cells. The simulation results pertain to analog behavior and the same are presented.

5.1 Memristor Materials: Working Conditions and Properties

Most of the memristors operate in the voltage range up to 2V with few exceptions wherein the range goes to 50V. Similar behavior is observed for the memristor operating current which is almost negligible i.e., 0.25µA for Cu/SiO_2/Pt memristor. The normal current range is up to 10 mA for Pt/Fe_2O_3/Pt memristor. However, the Pt/GO/ITO and ITO/HCuPc/Ti memristor requires the current of 100 mA to fall in memristive domain. The operating power is dependent on the operating current and voltage of the device and it can be seen it varies from 0.5µW to 800mW. These variations can be attributed to the material and its capacity to fall in memristive domain. Depending on the operating power range memristors can be categorized into low, moderate and high-power range, namely from 0.5 to 2.26µW, 75µW to 18mW and 225 to 800mW. The memristors which fall in first category are Cu/SiO_2/Pt, MNa, Au/SAM/Pd and TMJ. Memristors Pd/SAM/Pd, Pt/TiO_2/Pt, Ag/Si/p-type Si, Pt/NiO/Pt and Pt/Fe_2O_3/Pt fall in moderate power category and Au/PEDOT:SS/Au, VO2, Pt/GO/ITO and ITO/HCuPc/Ti are high power consuming memristor and falls in third and high-power consuming category. This is shown in Table 5.1 and graphically represented in Fig. 5.1.

Memristive phenomenon also reflects as memcapacitance and meminductance and show memcapacitive behavior in NEMS and PZT. NEMS and PZT respectively mean nanoelectronics mechanical systems and piezoelectric material. These devices utilize mechanical and electrical properties and present themselves as key components in (Radio Frequency) RF applications like such as impedance

matching circuits, tunable filters and voltage controlled oscillators. The nano-structure varies depending on the type of application intended which may be diaphragm, micro-bridge or cantilever-based structure apart from ReRAM and synapse. However, meminductive phenomenon is based on controlled change of geometry of the device and is named bimorph effect. Bimorph effect is temperature dependent. Meminductive devices find applications in frequency related applications like tuning and oscillators.

Table. 5.1 Values of memristor electrical parameters

Sr. No	Voltage (V)	Current (mA)	Power	Other Units	Material
1	2	0.00025	0.5 µW		CU/Sio_2/Pt
2	0.05	0.02	1 µW		MNa
3	1.5	0.001	1.5 µW		Au/SAM/Pd
4	0.65	0.00347	2.26 µW		TMJ
5	1.5	0.05	75 µW		Pd/SAM/Pd
6	2	0.2	400 µW		Pt/TiO_2/Pt
7	4	1.5	6 mW		Ag/Si/p-typeSi
8	1.5	5	7.5 mW		Pt/NiO/Pt
9	1.8	10	18 mW		Pt/Fe_2O_3/Pt
10	5	45	225 mW		Au/PEDOT:SS/Au
11	50	6	300 mW		VO2
12	6	100	600 mW		Pt/GO/ITO
13	8	100	800 mW		ITO/HCuPc/Ti
14	0-3	--	--	1.75-11.5pF	NEMS
15	-7 to +7	--	--	0.25-7.75pF	Pt/PZT/Pt
16	0 – 2	--	--	5-8.5nH	a-Si/Al

Table 5.2 represents classification of different memristors based on consumption of power

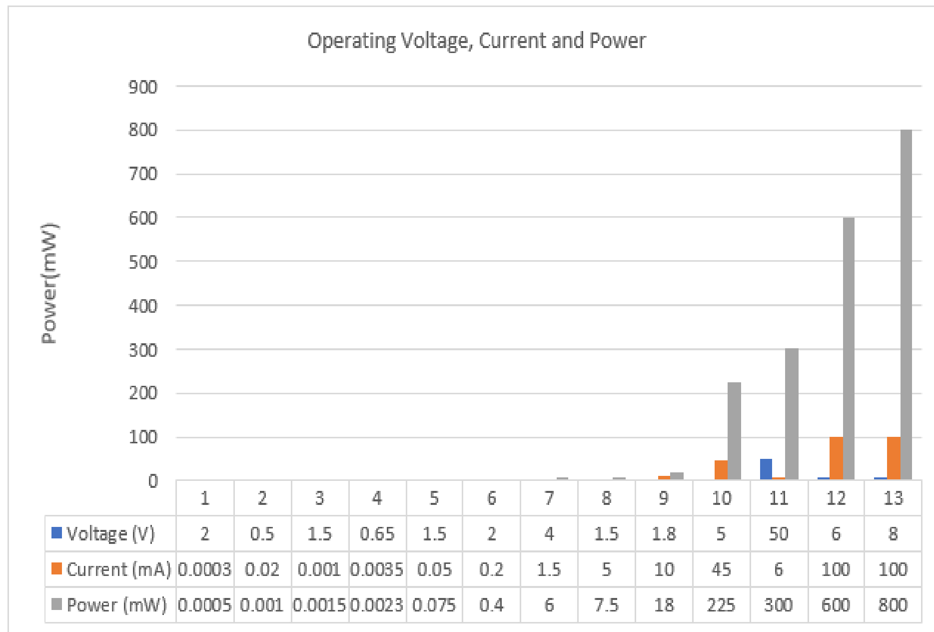


Fig. 5.1 Memristor operating voltage, current and power

Table 5.2 Segregation of memristors based on power consumption

0.5 – 2.26 μW	75 μW – 18mW	225 – 800mW
• $Cu/SiO_2/Pt$ • MnA • Au/SAM/Pd • TMJ	• Pd/SAM/Pd • $Pt/TiO_2/Pt$ • Ag/Si/p-type Si • Pt/NiO/Pt • $Pt/Fe_2O_3/Pt$	• Au/PEDOT:SS/Au • VO2 • Pt/GO/ITO • ITO/HCuPc/Ti

5.2 Phase Change Memory Cell

The Phase Change Memory (PCM) phenomenon between crystalline to amorphous and Metal – Insulator – Metal (MIM) and their application as ultra high density memory and related circuit/s have been described in detail earlier. This section describes the mathematics, SPICE simulation and results for both.

5.2.1 Phase Change Phenomenon SPICE Simulation

The PCM cell model uses threshold voltage and current to define switching. The switching of the model is based on crystalline factor C_x which swings between zero and one. Complete modeling of the PCM memory cell requires individual models of electrical resistance, computation of temperature, crystalline fraction and storage state. Thin film chalcogenide based PCM device is shown in Fig. 5.2 and is based on Joule heating.

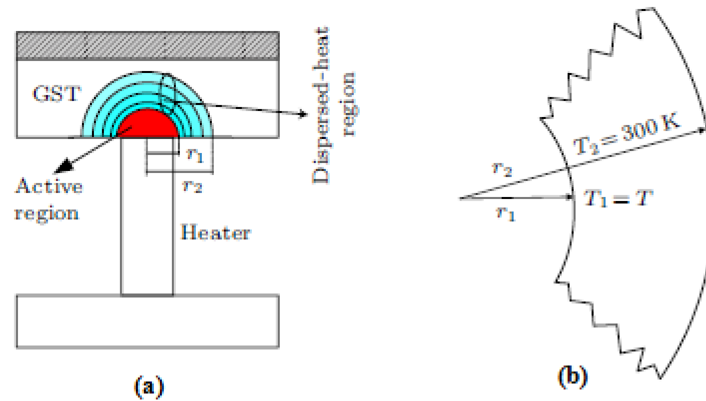


Fig. 5.2 (a) Physical model of PCM cell (b) Thermal model of PCM cell

Following equation describes the model of cell's electrical resistance.

$$R = (1 - C_x)R_a + C_x R_c \qquad (5.1)$$

Here, R_c/R_a= Resistive value of completely crystallized/amorphized cell respectively

C_x= crystalline fraction.

C_x= 1/0 means cell is in crystalline/amorphous state respectively.

R_c and R_a follow an temperature dependent Arrhenius law

$$R_a = R_{oa} \exp\left(\frac{E_a}{K_B T}\right) \qquad (5.2)$$

$$R_c = R_{oc} \exp\left(\frac{E_c}{K_b T}\right) \qquad (5.3)$$

Here

R_{oa} = Amorphous state's resistance coefficient

R_{oc} = Crystalline state's resistance coefficient

E_a = Activation energy: Amorphous state

E_c = Activation energy: Crystalline state

K_B = Boltzmann's constant

T = Temperature.

The working of the thermal physical model of the PCM cell depicted in Fig. 5.2 is as described. The potential difference results into power density in the PCM cell which in turn governs its temperature. Temperature is highest/maximum at the phase change layer's bottom portion. Top electrode's large surface area dissipates more heat compared to the bottom electrode with comparatively less surface area. Dispersed heat region and active region of the phase change memory cell together comprises its thermal physical model.

Calculations are simplified by using following assumptions:

- Uniform distribution of temperature is considered in the active region
- Room temperature is considered at external periphery of heat dispersed region
- Constant temperature gradient is considered in heat dispersed region

Here: $T = T_1$ be the temperature of inner surface of heat dispersed region

T_2 = Room temperature of outer surface of heat dispersed region

Hence Q (Total heat flux) is given as:

$$W_d = Q = -\sum k\Delta T = \frac{2\pi k(T-300)r_1 r_2}{r_2 - r_1} \qquad (5.4)$$

Where

k = Thermal conductivity

ΔT = Temperature gradient outside active region

r_1 = Active region's radius of the PCM cell

r_2 = Radius of PCM cell (equivalent to thickness of GST cell)

Joule heating W_j and dispersed heat W_d together evaluates the temperature of PCM cell.

$$T = \int_{t0}^{t1} \frac{W_j - W_d}{C \times V} \tag{5.5}$$

Where

C = Phase change material's thermal capacity

V = PCM cell's active region volume

W_j is given by

$$W_j = I_R \times V_R \tag{5.6}$$

Where

I_R = Current across active region

V_R = Voltage across active region

The solution of eq. (5.2) can be derived to eq. (5.7) below by substituting W_d of equation (4) and W_j of eq. (5.6) in eq. (5.5) keeping in mind that Bottom End Electrode (BEC) squanders approximately 30% of total heat.

$$T = \frac{0.7\, W_j (r_2 - r_1)}{2\pi k r_1}\left(1 - \exp\left(-\frac{3kr_2}{(r_2 - r_1) r_1^2 C} t\right)\right) + 300 \tag{5.7}$$

Here

t = time and $T_m > T > T_x$

Where

T_x = GST material glass transition point temperature

T_m = GST material melting point temperature

Whilst applied temperature T is raised greater than the temperature of glass transition point T_m, the GST cell material starts to melt. Crystalline factor C_x switches during transition of the phase. The model parameters [103] are represented in Table. 5.3.

Table 5.3 PCM Model Parameters

Sign	Illustration	Unit
r_1	Active region's radius	50nm
r_2	PCM cell's radius	100nm
R_{oa}	Amorphous state's coefficient of resistance	1063
R_{oc}	Crystalline state's coefficients of resistance	289
E_a	Amorphous states' activation energy	0.15
E_c	Crystalline states' activation energy	0.05
C	$Ge_2Sb_2Te_5$ (GST) thermal capacity	$1.25 JcmK^{-1}$
K	$Ge_2Sb_2Te_5$ thermal conductivity	$4.63\times10^{-3} JcmK^{-1}S^{-1}$
V	PCM cell's volume	7×10^{-14} cm^3
T_x	Glass transition point temperature	200°C
T_m	Temperature corresponding to melting point	600°C

5.2.2 Phase Change Memory SPICE Model

The model is based on thermal and phase change processes. Crystalline fraction 'C_x' and Temperature 'T' are internal state variables. The mathematical definition is as represented.

$$I = R^{-1}(C_x, V_M)\, V_M \quad (5.8)$$

$$\frac{dT}{dt} = \frac{V_M^2}{C_h R\,(C_x, V_M)} + \frac{\delta}{C_h}\,(T_r - T) \quad (5.9)$$

$$\frac{dC_x}{dt} = \alpha\,(1 - C_x)\,\theta\,(T - T_x)\,\theta\,(T_m - T) - \beta C_x \theta\,(T - T_m) \quad (5.10)$$

Where

$$R(C_x, V) = R_{on} + (1 - C_x)\frac{R_{off} - R_{on}}{e^{\frac{V - V_t}{V_o}} + 1} \tag{5.11}$$

Here

I = Current

R = Resistance

C_x = Crystalline fraction

V_M = Voltage

C_h = Heat capacitance

δ = Dissipation constant

T_r = Ambient temperature

$\theta[.]$ = Step function

T_m = Melting point

T_x = Glass transition point

α = Constant for crystallization rate

β = Constant for amorphization rate

V_t = Threshold voltage

R_{on} & R_{off} = Limiting values of Memristance

V_o = Parameter responsible for shape of *V-I* curve

The model schematic is as represented in Fig. 5.3 which states that it is a second order current or voltage controlled memristive system.

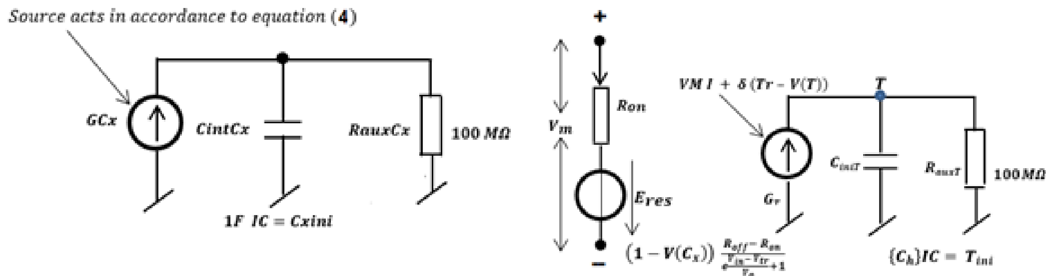


Fig. 5.3 Crystalline to Amorphous Phase Change SPICE Model

5.2.3 Description of SPICE Model

The eq. (5.8) to eq. (5.11) describes the thermal and phase change processes. The internal state variables crystalline fraction 'C_x' and temperature 'T' are taken into account. The condition $(T > T_m)$ and $(T_m > T > T_x)$ is responsible for crystallization and amorphization of the PCM cell. The comprehensive final model representing the phase change memory comprises of three sub-models i.e., the resistive port, and models computing the crystalline factor 'C_x' and temperature 'T'. The transient analysis of PCM cell based on the eq. (5.16) to eq. (5.19) is simulated using SPICE programming. The simulation output is shown in form of transient analysis in Fig. 5.4.

Duration of transient analysis is 660ns, which shows that by application of 4V pulse for duration of 330ns, the GST materials attains a temperature of 345°C, sufficient enough to crystallize. On similar lines, by applying 6V pulse for duration of 110ns, the material temperature reaches to 755°C and passes to amorphous state.

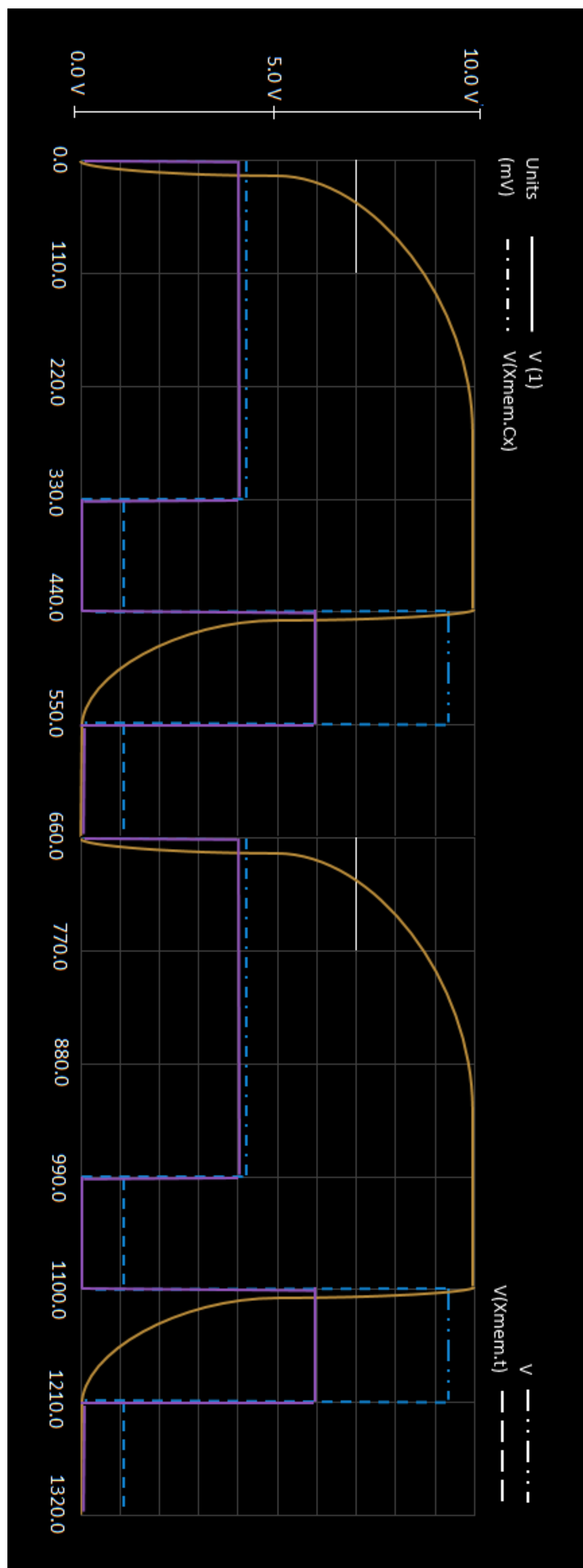


Fig 5.4 Transient analysis of PCM cell

When material is in crystalline phase, the crystalline factor attains the value ‘1 and 0’ when the state changes to amorphous. The Joule heating based reversible process is controlled by the electric pulse which further controls the amount of current in the cell which is liable for heating. The applied voltage and hence the amount/magnitude of current which may flow in the cell can be programmed indicating that heating can be controlled. This diversifies the resistance values of a single cell leading to very important concept – multibit storage ability for a single memory cell leading to direct application as super-ultra high-density nonvolatile memory. The PCM cell state is resistive and does not require external power source to maintain the state over time as that required in conventional charge based memories which further requires refresh circuits, indicating direct advantage like huge power savings and simple R/W and associated circuits.

5.3 Metal Insulator Transition

The phenomenon ‘Metal-Insulator transition’ denotes the process of sudden change in the conductivity behavior of the material based on change of certain parameters like stress, pressure, two dimensional system’s composition variation, magnetic field, gate voltage, etc [37].

With the detection of an electron a universal supposition came to fore in which it was understood that electrons move freely in metals in the influence of the electric field, whereas the case was opposite in case of nonmetals.

Hall Effect [98] considers one electron per atom as a standard order, with negligible dependence on temperature, to quantify the number of free electrons. Associated was the supposition that at any cost each atom of monovalent metal lost its outermost electron only.

Advent of Quantum Mechanics [99] proved instrumental in supplementing the reasonings to much need issues like trapping of electrons in chemical bonds or in closed shells of nonmetals. Based on quantum mechnics it explained that electrons

were not stuck or trapped in a ideal lattice. Each and every solutions of the Schrodinger equations meant intended for an electron subjected to an electronic potential field $V(x, y, z)$ namely presented by eq. (5.18) and eq. (5.19)

$$\nabla^2 + 2\left(\frac{m}{h^2}\right)(E - V)\psi = 0 \qquad (5.18)$$

Are of the form

$$\psi = e^{(ikr)}\, u\,(x, y, z) \qquad (5.19)$$

where u = episodic with the period of potential and represents an moving electron with wave number k and with no scattering. The solution of eq. (5.18) leads to spectrum of energy states separated into bands depicted in Fig. 5.5.

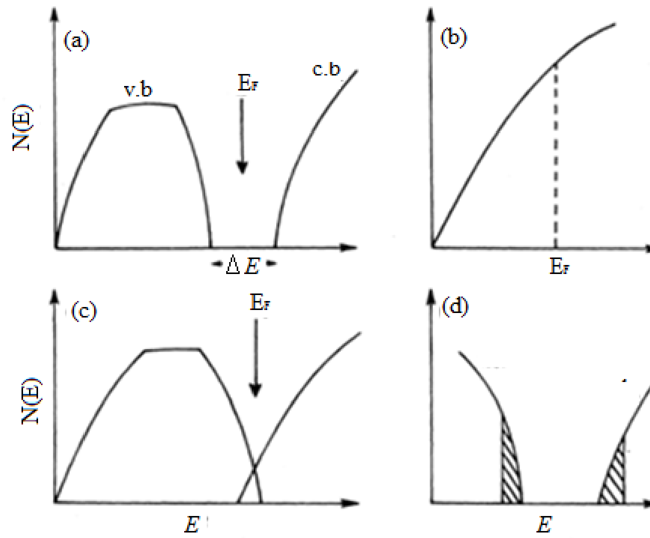


Fig. 5.5 State density of crystalline material. (a) Insulator, (b) Monovalent material, (c) Metal, (d) Electron-hole gas in insulator

Here

E_F = Fermi energy,

c.b. = Conduction band,

v.b. = Valence band.

ΔE = Energy difference

States that are occupied are shadowed.

In accordance with the principle of Pauli, states with the specified value of k can be occupied with only 2 electrons, so that for cubic structures, two electrons per atom will completely fill the first band. The material cannot conduct in the case wherein the first band is full and second empty as shown in Fig. 5.5 (a), not because the electrons are trapped or stuck, but because exactly as many electrons are moving from left to right as from right to left. This is clear experimentally, as well as from theory, because in crystalline nonmetals, if electrons are removed from the full valence band, the resultant 'positive hole' is mobile. The model makes clear why a sharp dissimilarity exists in nature between metallic and non-metallic behavior. In metals and in semiconductors with very heavy doping, the resistivity tends to finite value (or zero in superconductors) as the temperature tends to zero. In insulators it tends to infinity.

5.3.1 Metal to Insulator Phase Transition Memristive System

Previously, non-interacting electrons were confidently used to illustrate the dissimilarity among the metals and insulators. Afterwards electron-electron interaction $\left(\frac{e^2}{r_{12}}\right)$ was understood and introduced in to the problem and it was seen that free electron-gas crystallizes at low-densities and the in a low conducting state. One electron atom, cubic crystalline array with lattice parameter d is shown in Fig. 5.6. It was observed that for sufficiently large value of 'd' (which allows tunneling) the array behaved like an insulator and metallic for small values of 'd' indicative of metal-insulator transition with the condition $d > d_o$ the array is insulator and when $d < d_o$ it is a metal.

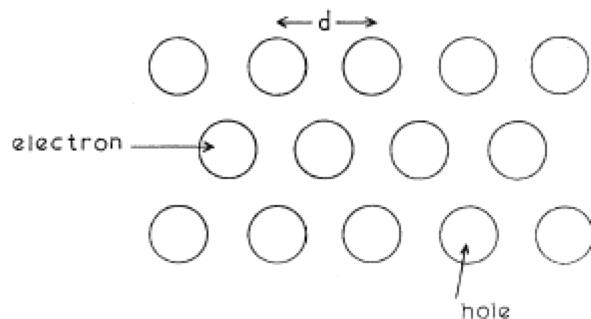


Fig. 5.6 Crystalline array of monovalent atoms

Current Controlled Negative Differential Resistance (CC-NDR) and S-Shaped Negative Differential Resistance (S-NDR) phenomenon are known as threshold switching under the influence of voltage bias displaying two stable states of resistance. Important switching i.e., threshold switching is owing to Joule heating resulting in filamentary metallic to insulator transition of phase. Remarkable plunge in resistance of the filamentary device resistance beyond bias threshold is observed. This is equivalent to a positive feedback that occurs owing to the fact that once a minute fraction of the device is Joule heated over the transformation temperature additional current flows all the way through this area further heating it thereby expanding the region. The metallic phase shows it presence until the current flow is occurring and vanishes when the bias is removed. This behavior makes the phase transformation volatile which is clearly different from memory switching which has the capacity to retain the resistive state over geological time periods after removal of the external bias. The uniqueness of the switching effect generates it applications in the areas like signal processing, buffer and isolation circuits providing compatibility with CMOS and hybrid circuits.

5.3.2 Metal-Insulator Phase Change SPICE Simulation Model

MIM phase transition cell model uses metallic fraction 'u', as an internal state variable. 'u' is represented in radial coordinates.

$$u = \frac{r_{met}}{r_{ch}} \qquad (5.12)$$

The model equations are

$$V = R_{ch}(u)I \qquad (5.13)$$

$$\frac{du}{dt} = \frac{1}{\left(\frac{d\Delta H}{du}\right)} \left(R_{ch}(u)\, I^2 - \Gamma_{th}\,(u)\, \Delta T\right) \qquad (5.14)$$

Where

$$R_{ch}(u) = \frac{1}{\frac{\rho_{ins}L}{\pi r_{ch}^2}\left[1 + \left(\frac{\rho_{ins}}{\rho_{met}} - 1\right) u^2\right]} \tag{5.15}$$

$$\Gamma_{th}(u) = \frac{1}{2\pi\, L\varsigma\left(\ln\frac{1}{u}\right)} \tag{5.16}$$

$$\frac{d\Delta H}{du} = \pi L r_{ch}^2\left[\hat{c}_p \Delta T\,\frac{1 - u^2 + 2u^2 \ln u}{2u\,(\ln u)^2} + 2\Delta\hat{h}_{tr} u\right] \tag{5.17}$$

Here

H = Enthalpy

Γ_{th} = Thermal conductance of the insulating shell

r_{met} = radius of metallic core

r_{ch} = conduction channel radius (30 nm)

ρ_{ins} = Insulating phase electrical resistivity (0.7×10^{-3} Ωm)

ρ_{met} = Metallic phase electrical resistivity (1×10^{-4} Ωm)

L = Conduction channel length (20 nm)

ҁ = Thermal conductivity (1.5 Wm^{-}1K^{-1})

ĉ = Volumetric heat capacity (2.6×10^{6}Jm^{-3}K^{-1})

$\Delta\hat{h}_{tr}$ = Volumetric enthalpy of transformation (1.6×10^{8} Jm^{-3})

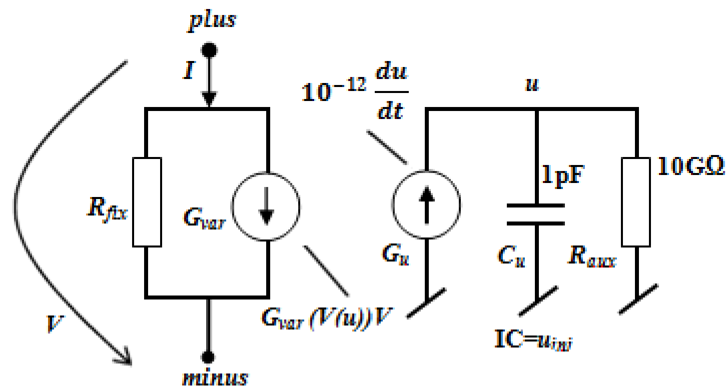


Fig. 5.7 Metal Insulator phase change SPICE model

The model represented in Fig. 5.7 transits its phase from insulator to metal with change in temperature. It falls in the category of memristor and is unipolar current controlled device. The SPICE model realizes

- Device's dynamic behavior which includes all complexities
- Switching at sub-nanosecond times

Eq. (5.16) and eq. (5.17) contains

- Logarithm of the phase composition state variable *u*
- Division by *u*
- Division by logarithm of *u*

u can attain values '0 and 1' making the equations unsolvable. To allow computation these equations can be rewritten in SPICE environment as follows:

$$I = R_{fix}^{-1} V + G_{var}(u) V \qquad (5.18)$$

$$R_{fix} = \frac{\rho_{ins} L}{\pi r_{ch}^2} \qquad (5.19)$$

$$G_{var}(u) = \frac{\pi r_{ch}^2}{L} \left(\frac{1}{\rho_{met}} - \frac{1}{\rho_{ins}} \right) u^2 \qquad (5.20)$$

Fig. 5.8 describes the transient analysis of the negative differential switch which is current controlled. The figure depicts simulation results of state variable's phase composition and that of the current.

Fig. 5.9 is the expanded view of the rising and falling edge depicting heating transient of 700 ps and a cooling transient of 2.3 ns respectively. The S-shape of the waveform makes the device and transition phenomenon to fall in memristive domain.

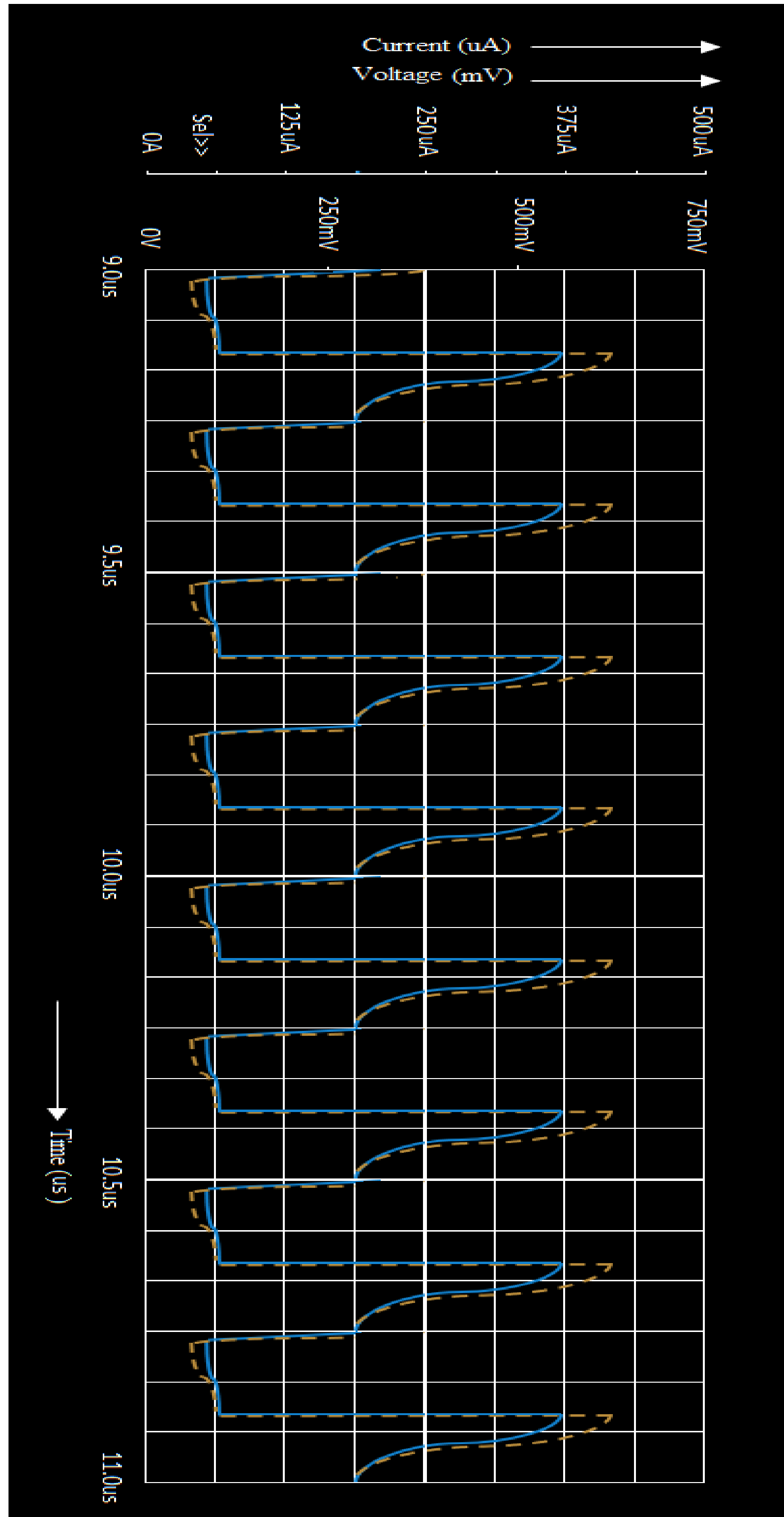


Fig. 5.8 Transient analysis of Metal-Insulator phase transition

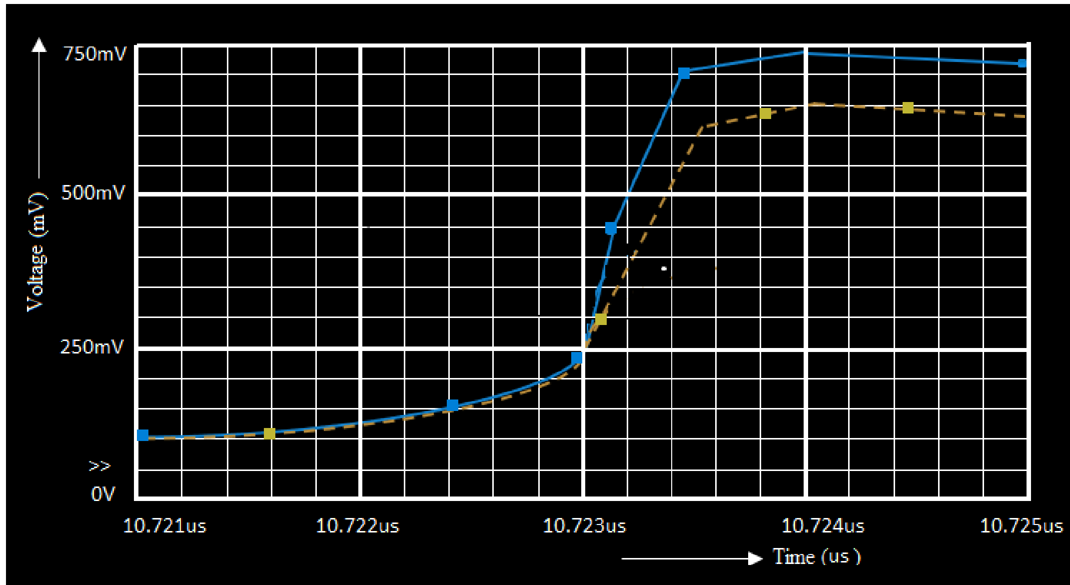


Fig. 5.9 Metal-Insulator S-Shape transient response

Summary

The chapter enumerates the memristor materials and their working conditions and properties, the operating electrical parameter values namely current, voltage and power. SPICE simulation of Phase Change and Metal-Insulator transition memory cells pertaining to analog behavior and the output is presented in terms of transient analysis.. The PCM phase change temperature observed are 345°C and 755°C for crystalline and amorphous phases respectively. Metal-Insulator phase change phenomenon is volatile and exists very small time duration of 700ps. Analysis of both the phase change processes indicates the applications over a very unique and comprehensive range.

CHAPTER – 6
DIGITAL SIMULATION

The chapter details about simulation and design outcomes in digital domain with respect to PCM cell and arrays of different sizes. The chapter describes the simulation and synthesis results of the adaptive algorithm for the PCM array and its realization in form of a FPGA chip. Verification of the functionality of the synthesized chip was carried out through an experimental set up that used Virtex-5 FPGA for synthesis purpose which was further supported by Xilinx Integrated System Environment (ISE) is included in this chapter. Also, the chapter enumerates and provides the procedure to mitigate the issues related with non-binary storage of information in the memory cell. It is a central and vital reason responsible for reducing the total per bit cost thereby escalating the competitiveness of PCM cell technology in nonvolatile memory market segment.

Issues related to non-binary information storage are as follows:

- Low latency programming
- High endurance capability when subjected to large programming cycles
- Low overall energy consumption
- Process and material variability
- Different temperature profiles reached in individual cells within the active storage region
- Reaching to different resistance values for same programming variables: voltage and current

Above points infers that programming using single pulse is not a practicable choice for MLC storage.

Methodology includes sophisticated schemes to program multi-level PCM storage. Technique includes iterative write and verify algorithms that exploits inimitable

programming distinctiveness of PCM in order to accomplish noteworthy improvements in the following:

- Density related to resistance level packing
- Reduction in cell variability
- Latency of programming
- Per bit energy
- Capacity of cell to store

Additionally, accurate program open paths for MLC storage by achieving several intermediate levels of resistance in between the RESET (high resistance) and SET (low resistance) states.

Fig. 6.1 denotes PCM cell's circuit schematic that constitutes of the active and phase-change element trapped amid a top and bottom electrode. Also, depicted is a memory cell array wherein FET acts as the selection device for individual cell.

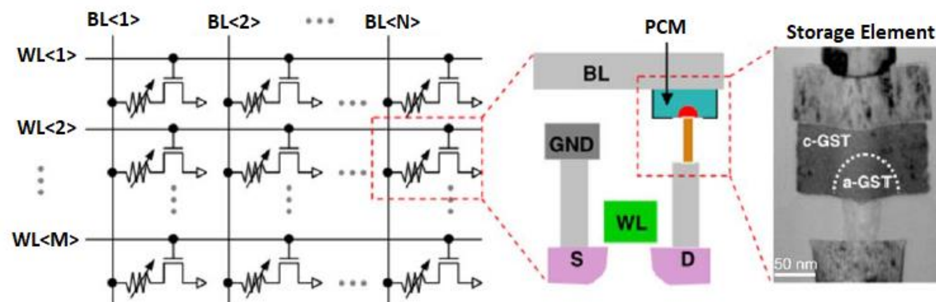


Fig. 6.1 Schematic of PCM cell array

6.1 Xilinx and Modelsim Simulation of PCM Cell

The simulation results of PCM cell is carried out on Xilinx ISE 14.7 software. It includes the RTL level simulation of the memory unit, its internals schematic and its block representation. The RTL level diagram presents the details of the memory chip with its pins details and internal schematic presents the diagram with internal

logic as flip-flops, registers, gates etc. Fig.6.2 shows the RTL view of PCM cell simulated in Xilinx ISE 14.7 software and table 6.1 lists the pin details.

Table 6.1 Pin detail of PCM cell

Pin	**Direction**	**Details**
Address_WL_BL<15:0>	Input	It denotes the PCM cell address based on row and column processing as word line and bit line respectively. It can be either Address_WL_BL = ‘0’ or Address_WL_BL = ‘1’.
Data_in (7:0)	Input	It presents the 8-bit data input of the memory cell
Data_out (7:0)	Output	It presents the 8-bit data output of the memory cell
Write (1-bit)	Input	It is the control signal input to write the data in memory. When Write = ‘1’, then contents are written into memory cell.
Read (1-bit)	Input	It is the control signal input to read the data from memory. When Read = ‘1’, then contents are read from memory cell.
Clk (1 bit)	Input	It presents the clock signal input with positive edge of the clock with 50 % duty cycle.
Reset (1 bit)	Input	It is the reset input used to keep the data_out as zero when reset signal is enabled.

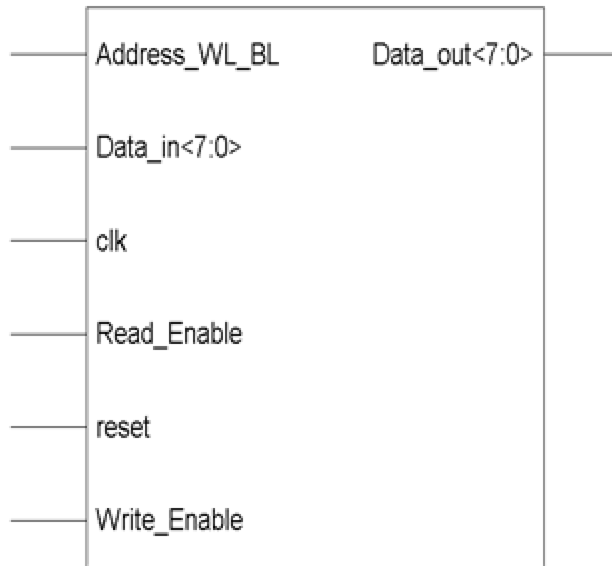


Fig. 6.2 RTL view of PCM cell

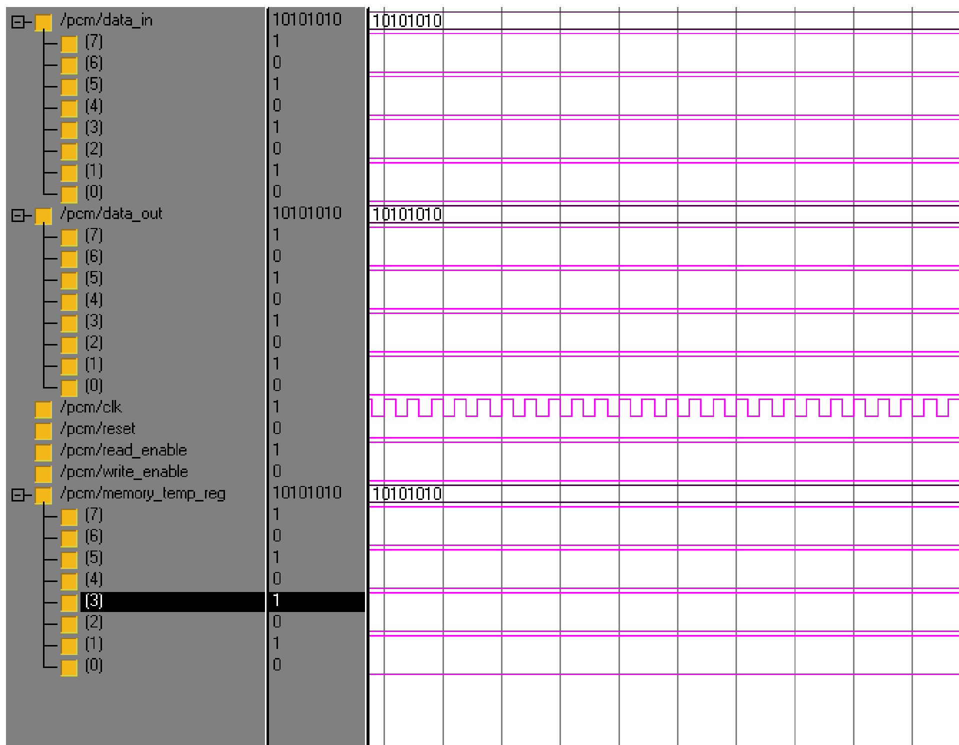


Fig.6.3 Modelsim simulation of PCM cell

The functional simulaion of PCM cell is done in Modelsim 10.1 software. The simulation test case desciption is depicted in Fig. 6.3.

The Modelsim simulation has the rising edge of clock signal which is synchronized with the reset input of the chip. The test case of the Modelsim simulation consists of Data_in <8 bit>, address_WL_BL <2 bit>, data out <8 bit>, and memory_temp_reg <8 bit>. The read and write are control signals in the test bench. When address_WL_BL = ‘0’, the data is read and written in temporary register and data_out pin of the chip. In the same way, when address_WL_BL = ‘1’, the data is read and written in temporary register and data_out pin of the chip. In the simulation waveform, the data_input = “10101010” and data_out = “10101010” and memory_temp_reg =”10101010”.

Test Case:
When, Data_in = “10101010”, Address_WL_BL <1:0> = ‘0’, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “10101010”.

When, Data_in = “10101010”, Address_WL_BL <1:0> = ‘0’, Write = ‘0’, Read = ‘1’, then Data_out = “10101010” and memory_temp_reg = “10101010”.

When, Data_in = “10101010”, Address_WL_BL <1:0> = ‘1’, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “10101010”.

When, Data_in = “10101010”, Address_WL_BL <1:0> = ‘1’, Write = ‘0’, Read = ‘1’, then Data_out = “10101010” and memory_temp_reg = “10101010”.

6.2 Xilinx and Modelsim Simulation of PCM Array

The RTL simulation of the PCM array (2 x 2) is shown in Fig. 6.4. The functional simulation for the same is depicted in Fig. 6.5. In the same way, The RTL simulation of the PCM array (4x4), (64x64) and (256x256) are shown in figures 6.6, 6.8 and 6.10 in that order. The functional simulation for the designed chip is depicted in figures 6.7, 6.9 and 6.11 respectively. The table 6.2 presents the

description of the pins utilized in the design that supports the complete functionality of the chip in ISE. The description of simulation waveforms is specified in test case-1, test case-2, and test case-3 respectively.

Table 6.2 Pin detail of PCM Array

Pin	**Direction**	**Details**
Address_WL_BL<15:0>	Input	It denotes the PCM cell address to identify the specific cell in array based on row and column processing as word line and bit line. It can be WL<N-bit> and BL<N-bit> based on address selection logic. In the design the maximum length is considered of 16 bit in which 8-bit are for row and column address respectively.
Data_in (7:0)	Input	It presents the 8-bit data input of the memory cell array against individual cell selected based on Address_WL_BL.
Data_out (7:0)	Output	It presents the 8-bit data output of the memory cell array against individual cell selected based on Address_WL_BL.
Write (1-bit)	Input	It is the control signal input to write the data in memory array. When Write = ‘1’, then contents are written into memory array.
Read (1-bit)	Input	It is the control signal input to read the data from memory. When Read = ‘1’,

		then contents are read from memory array.
Clk (1 bit)	Input	It presents the clock signal input to provide the positive edge of the clock with 50 % duty cycle.
Reset (1 bit)	Input	It is the reset input used to keep the data_out as zero when reset signal is enabled.

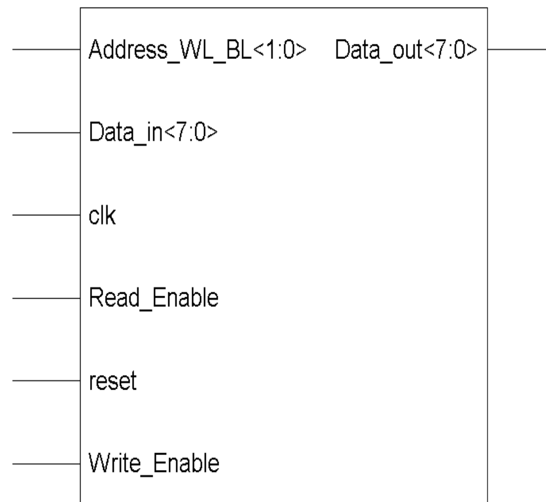
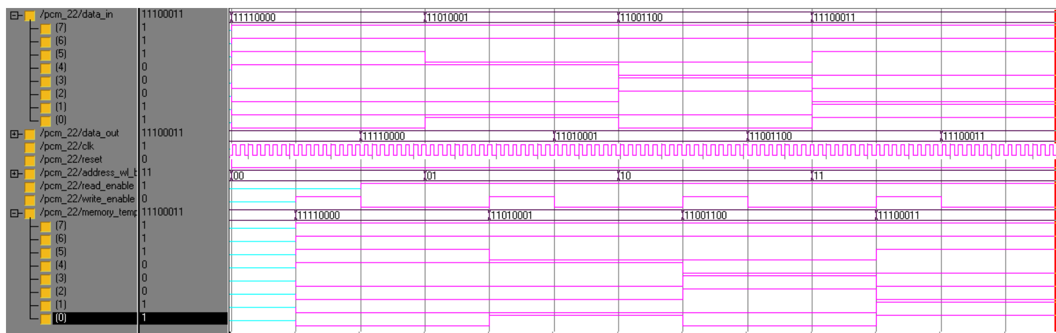
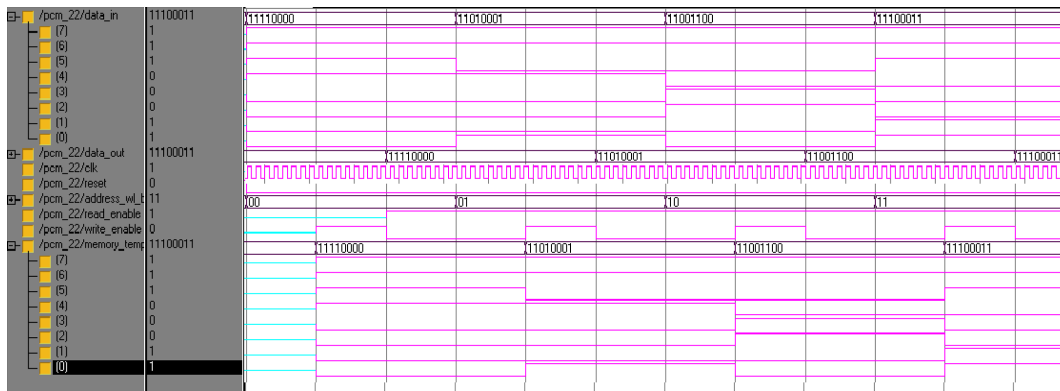


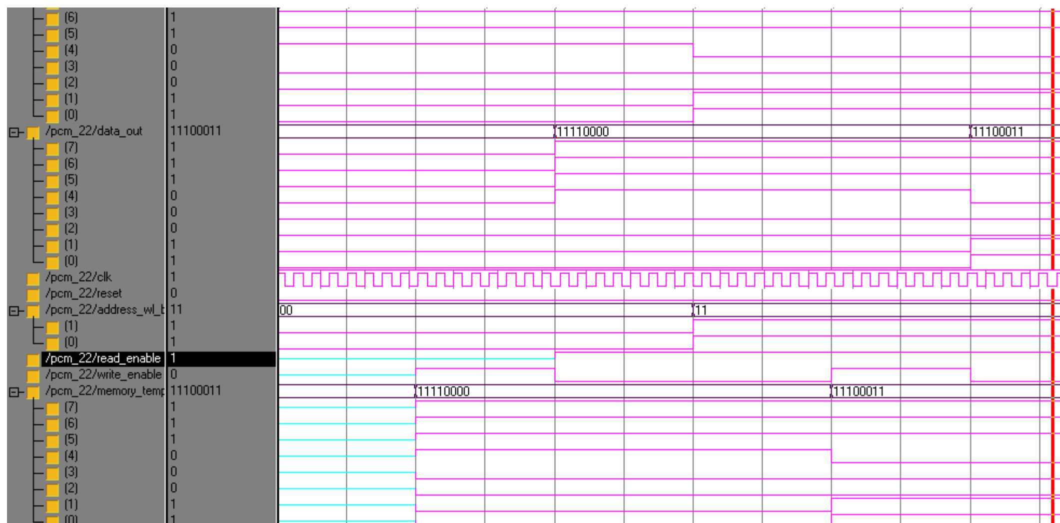
Fig. 6.4 RTL view of PCM array (2 x 2)



(a) Modelsim simulation of PCM array (2×2) in write mode



(b) Modelsim simulation of PCM (2×2) in read mode



(c) Modelsim simulation of PCM (2×2) in write/read mode

Fig. 6.5 Modelsim simulation of PCM array (2 x 2)

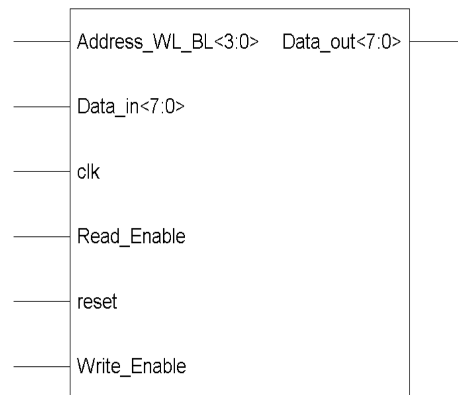


Fig. 6.6 RTL view of PCM array (4 x 4)

Fig. 6.7 Modelsim simulation of PCM array (4 x 4)

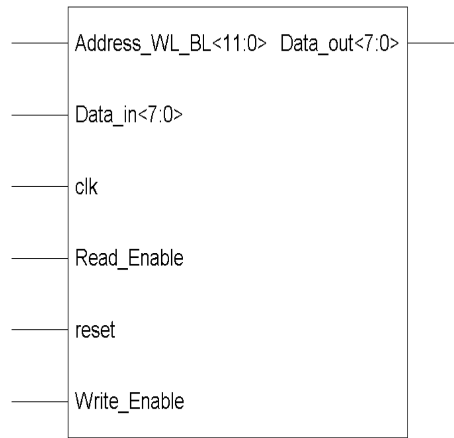


Fig. 6.8 RTL view of PCM array (64 x 64)

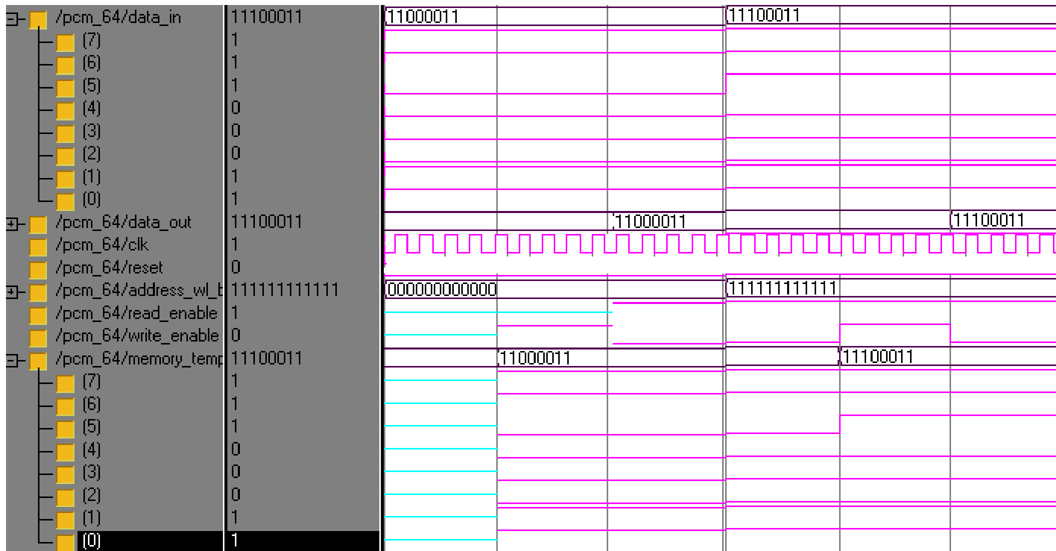


Fig. 6.9 Modelsim simulation of PCM array (64 x 64)

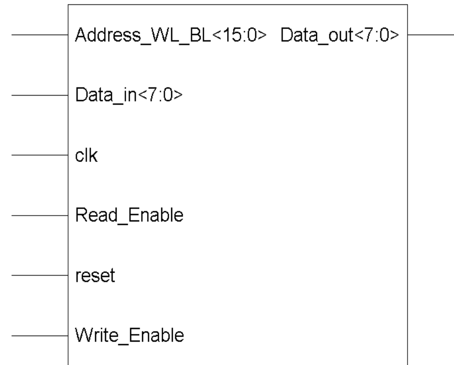


Fig. 6.10 RTL view of PCM array (256 x 256)

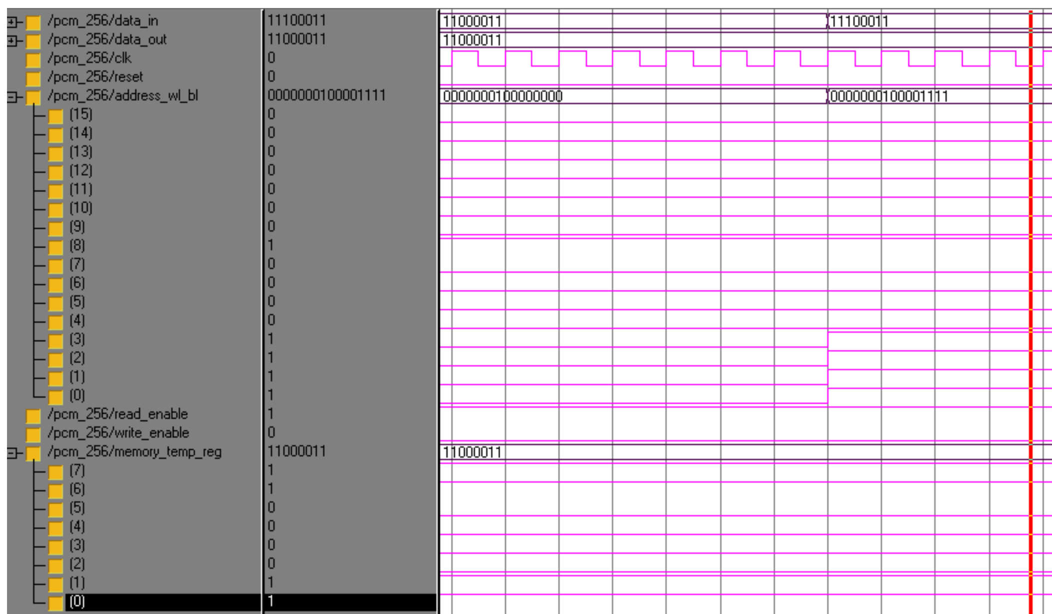


Fig. 6.11 Modelsim simulation of PCM array (256 x 256)

Test Case -1 PCM Array (2 x 2)

When, Data_in <7:0> = “11110000”, Address_WL_BL <1:0> = “00”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11110000”.

When, Data_in = “11110000”, Address_WL_BL <1:0> = “00”, Write = ‘0’, Read = ‘1’, then Data_out = “11110000” and memory_temp_reg = “11110000”.

When, Data_in <7:0> = “11010001”, Address_WL_BL <1:0> = “01”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11010001”.

When, Data_in = “11010001”, Address_WL_BL <1:0> = “01”, Write = ‘0’, Read = ‘1’, then Data_out = “11010001” and memory_temp_reg = “11010001”.
When, Data_in <7:0> = “11001100”, Address_WL_BL <1:0> = “10”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11001100”.
When, Data_in = “11001100”, Address_WL_BL <1:0> = “10”, Write = ‘0’, Read = ‘1’, then Data_out = “11010001” and memory_temp_reg = “11001100”.
When, Data_in <7:0> = “11100011”, Address_WL_BL <1:0> = “11”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11100011”.
When, Data_in = “11100011”, Address_WL_BL <1:0> = “10”, Write = ‘0’, Read = ‘1’, then Data_out = “11100011” and memory_temp_reg = “11100011”.

Test Case -2, PCM Array (4 x 4)

When, Data_in <7:0> = “00001111”, Address_WL_BL <3:0> = “0100”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “00001111”.
When, Data_in <7:0> = “00001111”, Address_WL_BL <3:0> = “0100”, Write = ‘0’, Read = ‘1’, then Data_out = “00001111” and memory_temp_reg = “00001111”.
When, Data_in <7:0> = “11110000”, Address_WL_BL <3:0> = “1111”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11110000”.
When, Data_in <7:0> = “11110000”, Address_WL_BL <3:0> = “1111”, Write = ‘0’, Read = ‘1’, then Data_out = “11110000” and memory_temp_reg = “11110000”.

Test Case -3, PCM Array (64 x 64)

When, Data_in <7:0> = “11000011”, Address_WL_BL <11:0> = “000000000000”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11000011”, Address_WL_BL <11:0> = “000000000000”, Write = ‘0’, Read = ‘1’, then Data_out = “11000011” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11100011”, Address_WL_BL <11:0> = “111111111111”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11000011”, Address_WL_BL <11:0> = “111111111111”, Write = ‘0’, Read = ‘1’, then Data_out = “11000011” and memory_temp_reg = “11000011”.

Test Case -4, PCM Array (256 x 256)

When, Data_in <7:0> = “11000011”, Address_WL_BL <15:0> = “0000000000000000”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11000011”, Address_WL_BL <15:0> = “0000000000000000”, Write = ‘0’, Read = ‘1’, then Data_out = “11000011” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11100011”, Address_WL_BL <15:0> = “0000000000001111”, Write = ‘1’, Read = ‘0’, then Data_out = “00000000” and memory_temp_reg = “11000011”.

When, Data_in <7:0> = “11000011”, Address_WL_BL <15:0> = “0000000000001111”, Write = ‘0’, Read = ‘1’, then Data_out = “11000011” and memory_temp_reg = “11000011”.

6.3 Xilinx and Modelsim Simulation of Adaptive Algorithm for PCM Array

Fig. 6.12 shows *V-I* characteristic during programming of the PCM cell between RESET and SET state. For applied voltage the change in current is nonlinear. At critical voltage snap-back takes place and the cell switches to dynamic, highly conductive ON state. The phenomenon is threshold switching and responsible factor to enable resistive the programming of the memory cell. In SET/ON

condition the conductivity is very high hence by appropriate Joule heating and subsequent quenching process the programming (phase switching) can be achieved. This is also synonymous of achieving the "Write" operation.

Voltages below threshold switching depicts RESET/OFF condition and are responsible for "Read" operation. The *V-I* curve also depicts the programming space for multilevel storage by quantifying the change of the resistance of the cell as a function of the programming current or the voltage.

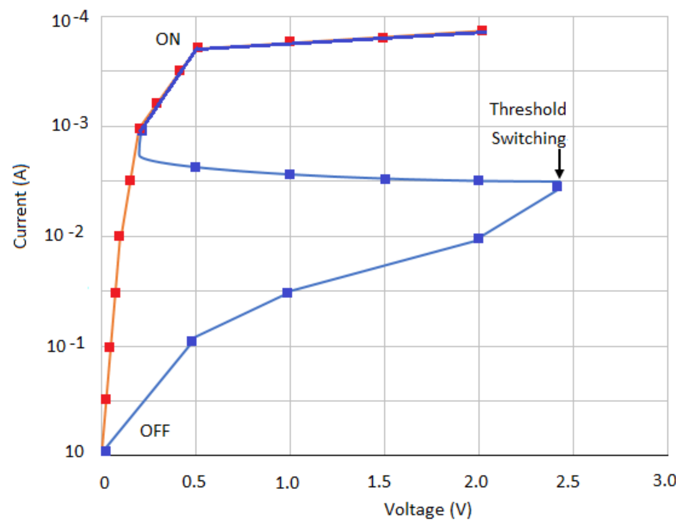


Fig. 6.12 *V-I* characteristics of PCM cell

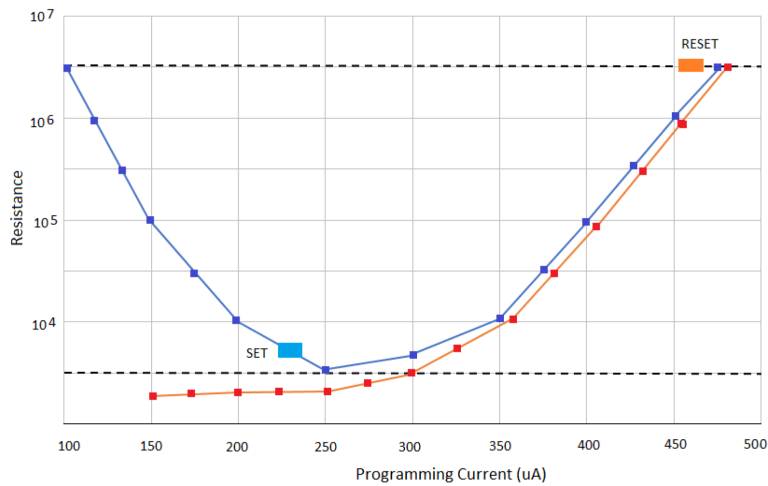


Fig. 6.13 Programming curve dependent on resistance difference

Fig. 6.13 depicts the characteristic programming curve as a resultant of rectangular programming pulses of growing amplitude, when programming begins from either RESET or the SET state.

6.3.1 Adaptive Algorithm

Fig. 6.14 illustrates the concept of iterative programming involving a sequence of program and verification logic.

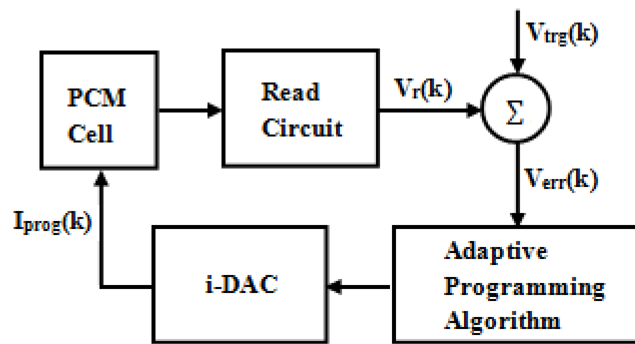


Fig. 6.14 Adaptive iterative programming procedure

RESET pulse is first applied followed by pulses that melt but of varying amplitude in the partial-RESET regime that are used to either augment or diminish the resistance. A verify step is performed after each programming pulse and the assessment of value of the state of the cell programmed in the preceding iteration is read. The programming current applied to the PCM cell in the subsequent iteration using the current digital-to-analog converter (i-DAC) is adapted according to the sign or the value of the error between the target level and read value of the cell state. The programming sequence ends when the error between the target level and the programmed state of the cell is smaller than a desired margin or when the maximum number of iterations has been reached.

Fig. 6.15 represents the flowchart to support the functionality of iterative programming. Procedure to characterize the reliability of the PCM prototype chip

is in terms of data retention and cycling endurance under variable time and temperature conditions. A sub-array of (256 × 256) pristine memory cells is selected to be subjected to 1 million RESET/SET cycles.

During cycling, short RESET/SET pulses are used compared to pulses used for MLC programming. The cycling RESET pulse is a box shaped pulse of maximum power. The cycling SET pulse is of reasonable power. At regular intervals cycling stops and the cells under test are tested in terms of MLC programming and data retention under variable time and temperature profiles. To assess the under practical operating conditions and to study the drift behavior at elevated temperatures, a profile in which the temperature is varied between 35°C and 85°C was used. This procedure continues for a total of 10^6 cycles.

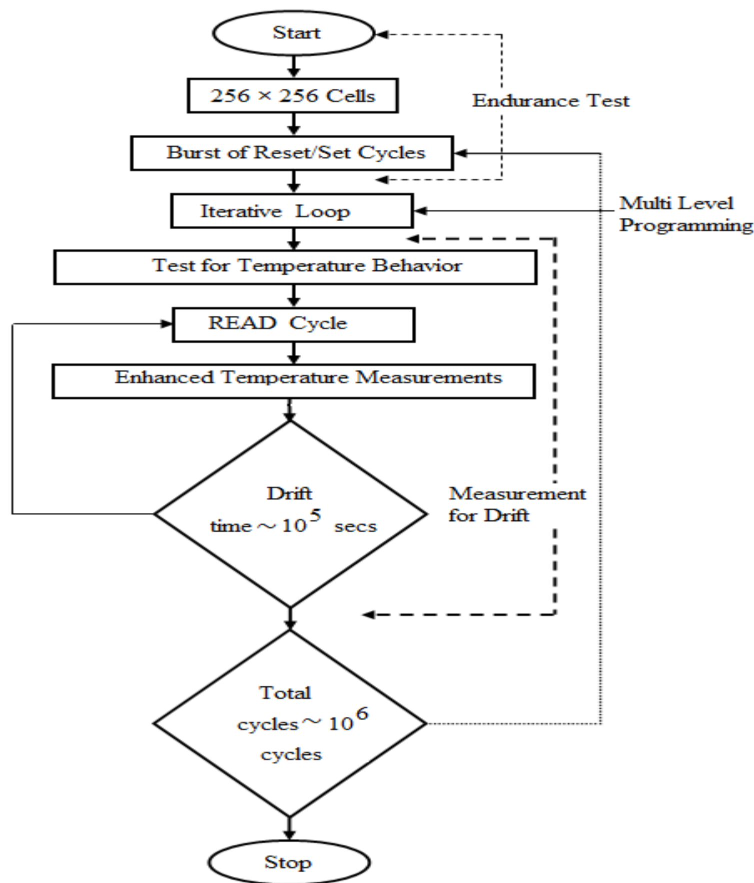


Fig. 6.15 Flowchart of the experimental procedure

The Fig. 6.16 depicts the RTL view of the adaptive algorithm designed in Xilinx SE.

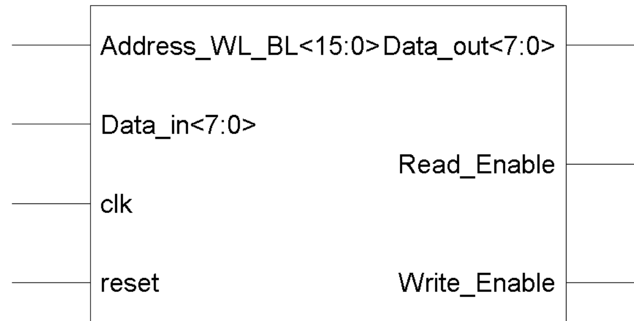


Fig. 6.16 RTL view of PCM temperature profile

Table 6.3 Pin details of adaptive algorithm chip for R/W operation and temperature variation.

Pin	**Direction**	**Details**
Address_WL_BL<15:0>	Input	It denotes the PCM cell address to identify the specific cell in array based on row and column processing as word line and bit line. It can be WL<N bit> and BL<N bit> based on address selection logic. In the design the maximum length is considered of 16 bit in which 8-bit are for row address and 8-bit are column address.
Data_in (7:0)	Input	It presents the 8-bit data input of the memory cell array against individual cell selected based on Address_WL_BL.
Data_out (7:0)	Output	It presents the 8-bit data output of the memory cell array against individual

		cell selected based on Address_WL_BL.
Write (1-bit)	Inout	It is the control signal input to write the data in memory array. When Write = ‘1’, then contents are written into memory array.
Read (1-bit)	Inout	It is the control signal input to read the data from memory. When Read = ‘1’, then contents are read from memory array.
Clk (1 bit)	Input	It presents the clock signal input to provide the positive edge of the clock with 50 % duty cycle.
Reset (1 bit)	Input	It is the reset input used to keep the data_out as zero when reset signal is enabled.

The Fig. 6.17 presents the Modelsim simulation of read/write operation for approximately 10^6 cycles. The simulation is based on the Finite State Machine (FSM) concept in which one hot encoding method is used to process the states. The Fig. 6.18 presents Modelsim simulation of temperature profile of PCM Cell. The simulation is carried at 85^0C and read/write endurance is operation is analyzed for 1000399 cycles. The test case is presented to understand the simulation behavior.

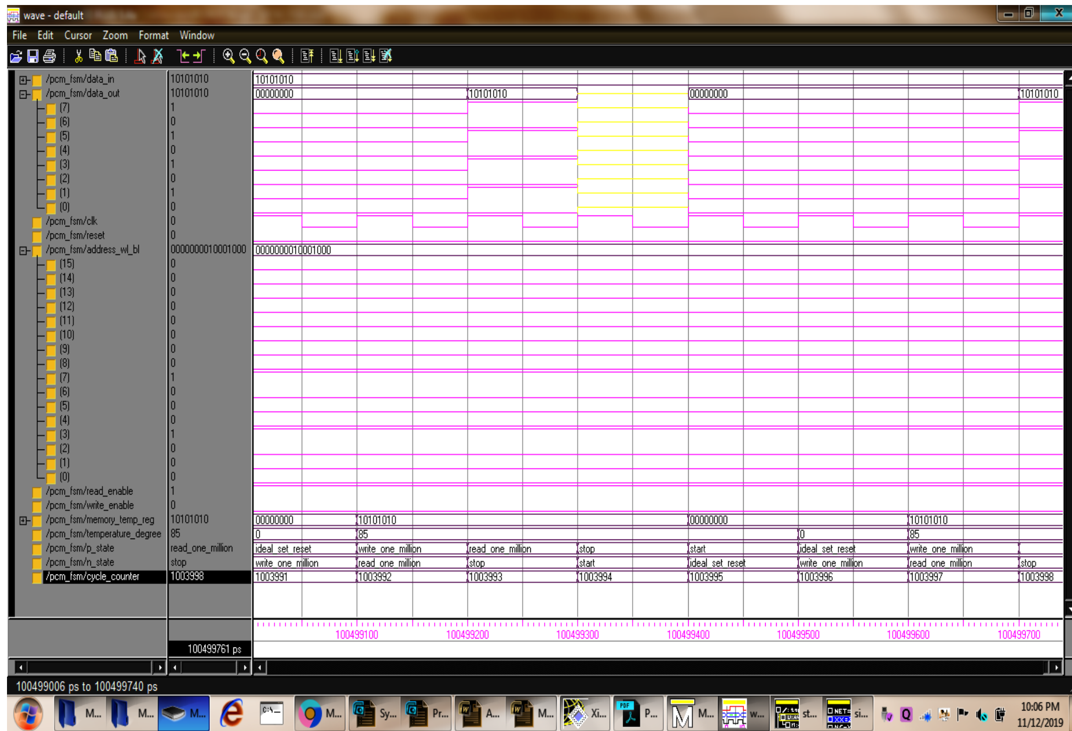


Fig. 6.17 Modelsim simulation of read/write operation ($\sim 10^6$) cycles

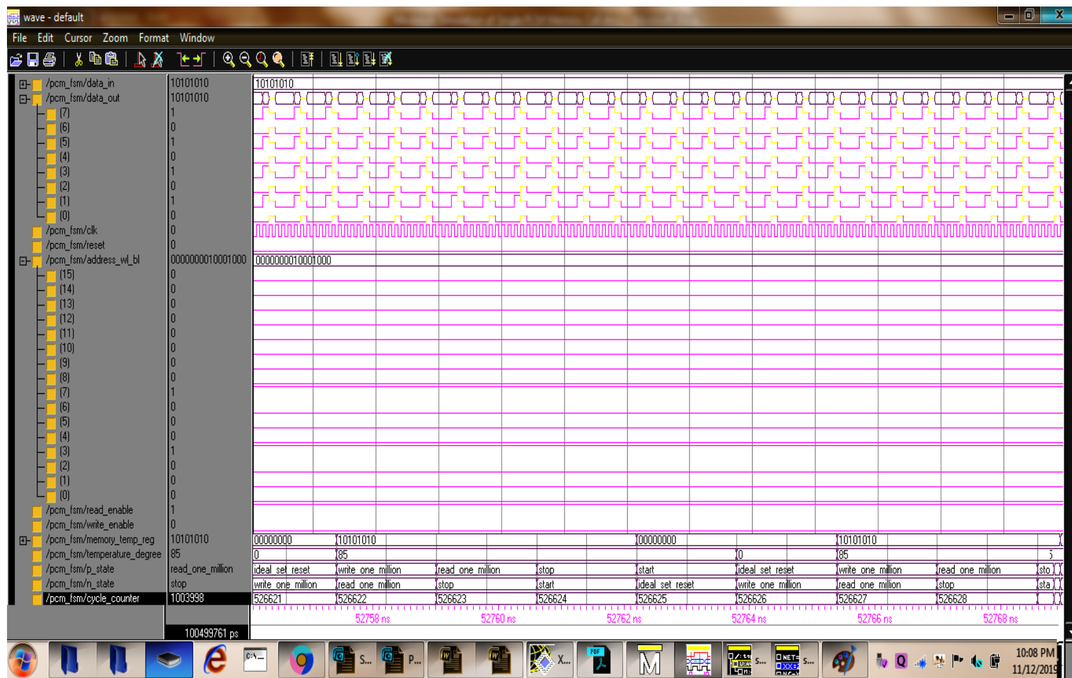


Fig. 6.18 Modelsim simulation of temperature profile of PCM Cell

Test Case – PCM Behavior in accordance to Adaptive Algorithm

When, Data_in <7:0> = "10101010", Address_WL_BL <15:0> = "0000000010001000", Write = '1', Read = '0', then memory_temp_reg = "10101010", temperature_degree = 85 (decimal) and endurance cycle (max) = 100399 (decimal).

When, Data_in <7:0> = "10101010", Address_WL_BL <15:0> = "0000000010001000", Write = '0', Read = '1', then Data_out = "10101010" and memory_temp_reg = "10101010", temperature_degree = 85 (decimal) and endurance cycle (max) = 100399 (decimal).

6.4 FPGA Verification

The synthesis method is done on Xilinx Virtex – 5 XC5VLX110T Digilent manufactured FPGA as shown in Fig. 6.19. It has two Xilinx XCF32P platform flash ROMs for storing large device configurations of 32 MByte each, 64 bits wide 256 Mbyte DDR2 modules compatible with Embedded Development Kit (EDK) supported IP and software drivers. It has in board 32-bit synchronous Zero Bus Turnaround (ZBT) SRAM and Intel P30 Strata Flash. It supports 10/100/1000 tri-speed Ethernet PHY supporting Media Independent Interface (MII), Gigabit Media Independent Interface (GMII), Reduced Gigabit Media Independent Interface (RGMII), and Serial Gigabit Media Independent Interface (SGMII), Universal Serial Bus (USB) host and peripheral controllers, programmable system clock generator. It has Stereo Audio Codec (SAC) 97 with line in, line out, headphone, microphone, and Sony/Philips Digital Interface Format (SPDIF) digital audio jacks, RS-232 port, 16 x 2 character LCD, I/O devices and ports.

Fig. 6.19 Functional view of FPGA Virtex – 5 FPGA

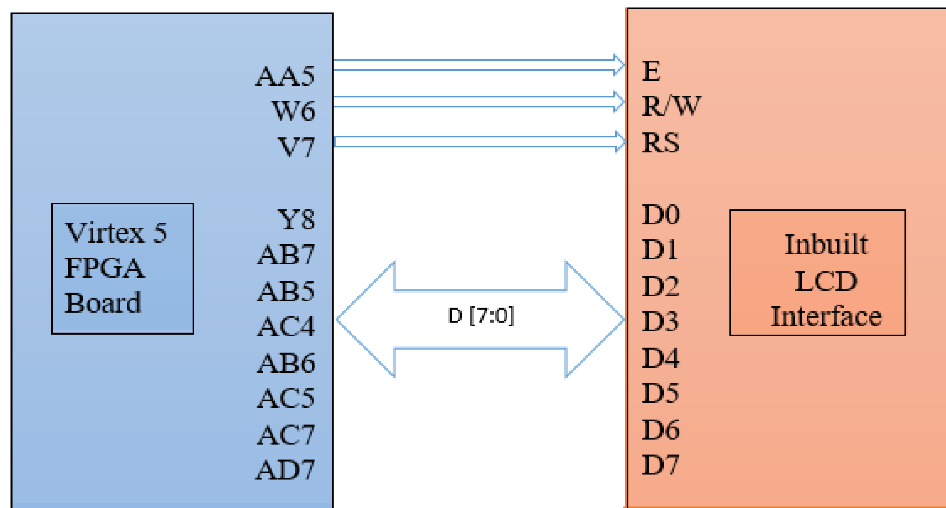


Fig. 6.20 LCD Interface of FPGA

In the synthesis procedure the program is burned in the ROM memory of FPGA. The Virtex-5 FPGA has inbuilt LCD controller and contains character-generator ROM (CGROM) with 208 fixed 5 × 8 character patterns, a character-generator RAM (CGRAM) used to hold eight user-defined 5 × 8 characters, and

one display data RAM (DDRAM) memory which can hold 80 character codes. The character codes are written into the DDRAM memory, which serves as the indexes into the CGROM (or CGRAM). The character code is written into the specific DDRAM memory location and it causes the related characters to appear at the consistent display location. The display locations are shifted to right side or to left side by setting one bit in the instruction register (IR). The IR register directs the LCD operations and direct display operations such as shift left or right, clear display, set DDRAM address. Fig.6.20 shows the interface diagram of the LCD (16 x 2) to Virtex 5 FPGA. The LCD unit is 16-pin connector in which pins 15 and 16 are not used and applicable for optional backlight. The remaining 14-pin interface has three control signals, eight data signals, and three voltage supply signals. The eight-bidirectional data bus signals interconnect data to the control registers or RAM locations. The RS (Register Strobe) signal clocks data into registers or into RAM, the R/W signal determines bus direction, and the E signal enables the bus for read or write operations. The user constraint file (UCF) is used to lock the FPGA pins. The details of the pins are given in table 6.4.

Table 6.4 UCF pin details in FPGA synthesis

Input Logic	**Pins**	**Description**
Clk	N15	Input clock pulse
RS	V7	It is the register select input, high for data, low for instructions.
R/W	W6	Read/write control signal: R/W= 1 for read, and R/W = 0 for write
E	AA5	Read/write enable input high for OE, falling edge writes data
DB0	Y8	Input data bit of bidirectional data bus 0
DB1	AB7	Input data bit of bidirectional data bus 1
DB2	AB5	Input data bit of bidirectional data bus 2

DB3	AC4	Input data bit of bidirectional data bus 3
DB4	AB6	Input data bit of bidirectional data bus 4
DB5	AC5	Input data bit of bidirectional data bus 5
DB6	AC7	Input data bit of bidirectional data bus 6
DB7	AD7	Input data bit of bidirectional data bus 7
Vss	Unassigned	It is the ground input
Vdd	Unassigned	5V input for power supply
Vo	Unassigned	Contrast voltage input (typically 100mV-200mV) at 20^0 C

Fig. 6.21 Experimental set-up

Fig. 6.21 present the experimental FPGA synthesis for 8-bit memory data and output observed on LEDs. Switches give the input of address_WL_BL, RESET, Read/Write and 8-bit data input. The LEDs are used as a display to validate the correctness of the data input for PCM array. The Data_in <7:0> = “10101010”,

Address_WL_BL <15:0> = "0000000010001000", Write = '1', Write/Read = '0', then LED display Data_out <7:0> = "10101010".

6.5 FPGA Parameters Analysis

The FPGA device utilization report has been taken form Xilinx ISE 14.7 directly. The report comprises the information of number of slices, number of slice registers, number of LUTs, number of flip-flops, memory utilization and blocks/(IoBs), The information is used to estimate the hardware resources utilization of FPGA for synthesis. If the resources utilization is greater than 100 %, then the designer has to change the design for synthesis on the same FPGA. Table 6.4 lists the detail of the hardware resources utilized on Virtex -5 FPGA for pre-synthesized code. The timing parameters of the same FPGA are listed in table 6.5. It presents the details of the timing information of combinational path delay and maximum frequency support for the configuration of FPGA device.

Table 6.5 Xilinx ISE hardware chip parameters for PCM array

Parameter	PCM	PCM (2 x 2)	PCM (4 x 4)	PCM (64 x 64)	PCM (256 x 256)
Slices Usage	16	16	16	16	16
Slice flip-flops	2	4	8	21	84
LUTs Usage	1	2	4	21	52
IoBs	20	22	26	32	36
GCLKs	1	1	1	1	1
Memory Usage (kB)	4551344	4551392	4551512	4552368	4552517

Table 6.6 Xilinx ISE timing parameters for PCM array

Parameter	PCM	PCM (2 x 2)	PCM (4 x 4)	PCM (64 x 64)	PCM (256 x 256)
Frequency (MHz)	1467.136	1467.136	1467.136	1467.136	1467.136
Combinational Delay (ns)	2.826	2.910	3.115	3.371	4.50

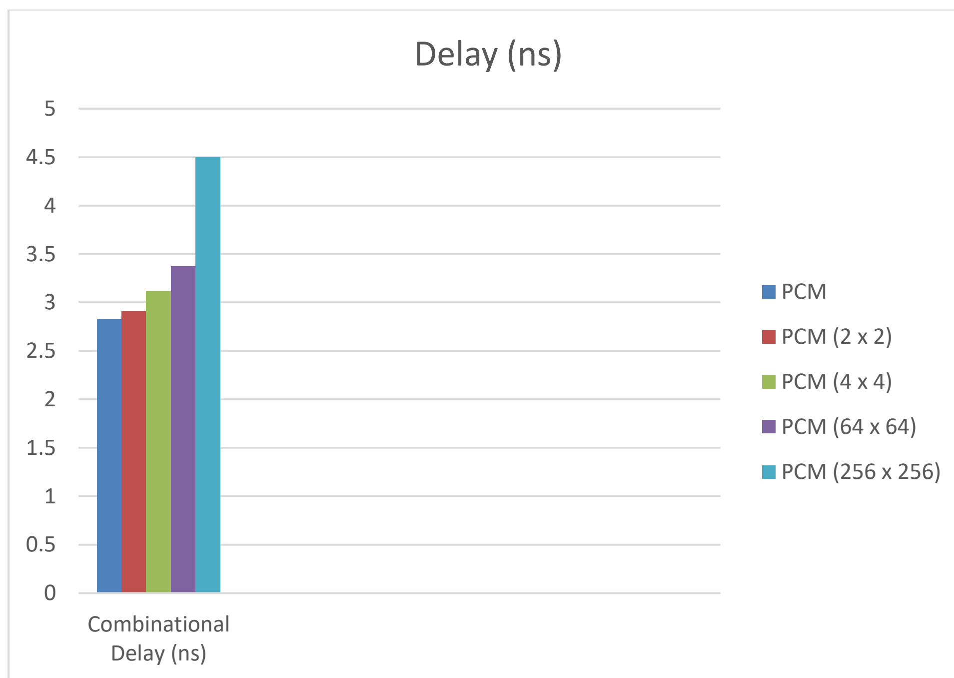


Fig. 6.22 Adaptive model for PCM temperature profile

Fig. 6.22 presents the comparative time graph for adaptive model for PCM temperature profile against different PCM configuration. It is clear from the graph the time delay is increasing as the cluster size of the chip is increasing. It is clear that the delay will increase with the increase in hardware utilization.

Table 6.7 presents the comparative analysis for PCM cell array endurance cycle and the convergence rate with the existing work based on iterative programming. It

supports the PCM endurance capability at 85°C for multi-bit level Read/Write operation. It is estimated that our work is an optimal solution in terms of endurance cycle and convergence rate for PCM array.

Table 6.7 Comparison with existing work

Parameter	Aravinthan Athmanathan *et al*. (2016) [100]	N. Papandreou *et al*. (2011) [101]	Proposed Work
Endurance Cycles	**10^6**	**10^6**	**1000399**
Convergence Rate	**99.0%**	**98.2%**	**99.25%**

The work represented is a simulation of behavior of PCM cell in digital domain. The outcome will impact the semiconductor industry from various aspects like reliability, endurance, resistance retaining capacity of the cell for multi-bit computations.

Summary

Mature and omnipresent digital domain provides versatile platform and ease to test and verify the claims of new technologies to verify their claim. Chapter summarizes a setup based on adaptive algorithm for simulation of PCM cell and arrays to verify various important parameters to prove the truth of the PCM technology. PCM cell array chip of different sizes were designed, simulated and verified on FPGA platform. The temperature profile was also simulated and tested for R/W operation and its endurance was tested for over one million cycles. It is a promising solution for further development of the technology.

CHAPTER – 7
CONCLUSION

The chapter presents the conclusions drawn from the research work and recommendations about scope for further research possibilities.

7.1 Conclusions

Nature and behavior of natural phenomenon is fundamentally analogous is nature while computation is surprisingly digital in nature and adopts a long path of conversions between analog and digital to derive the results. This process has delayed the practical realization of the idea – data computation while travelling on the data bus. If realized the computation capability will reach to an altogether different level with unimaginable applications possible. One example possible is brain on chip or chip on a brain.

In earlier days, operational amplifiers paved path for analog computations but suffered with many lacunas. Still lot is left to be done and one of the aspects is analog computing which is seeing the dawn owing to practical realization of Memristor.

However, present scenario is based on amalgamation and integration of best practices in the technological arena and has led the computation world to reach to the heights we see today wherein hardware and software complements each other nicely. In spite of this, some simple well known issues become the bottlenecks and hence hindrance in the future development of many applications. One such issue is von Neumann architecture wherein data transfer issues reduces the computation efficiency many folds. Another issue is computation based on binary number system while present computation scenario is mature for multi-level computations. This also calls for new logic implementation.

Memristor – the 4th fundamental device is capable to provide the solutions to present computation paradigm because it is capable of analog as well as digital

storage and computation. Additional feature includes multi level bit storage capability that too in resistive paradigm indicative of huge power savings and behavior as a synapse of a brain leading to direct applications as neuromorphic hardware. Unexplored aspects of various materials inherently at nano level, especially behavior as memristor and change of phase of the material, has come up as unique solution to current bottlenecks. This has also provided much needed lease to the existence of the Moore's law.

The research work includes

- Analysis of range of materials for memristive property
- Analysis of physical mechanisms responsible for memristive behavior
- Behavioral classification of memristor to memristive, memcapacitive and meminductive phenomenon.
- Operating voltage, current and power of different memristors
- Differentiation of memristors based on consumption of power
- Understanding of phase change phenomenon leading to memristor applications as ultra-high density nonvolatile memory
- Understanding of phenomenon leading to multi-level bit storage capability in resistive domain
- Simulation of memory cell in SPICE environment by modeling the reversible physical phenomenon responsible for
  - Crystalline to amorphous phase transition
  - Metal to Insulator phase transition
- Represents transition analysis of the memory cells based on the phenomenon cited in the point above
- In the research work the study of memristor is done successfully in both the analog and the digital domain.
- The simulation of Phase change memory is done in analog and digital domain. Transient Analysis of Spice Memristive Phase Change Model. The transient analysis is for duration of 660 ns.

- The multibit operation and multi-array PCM cell chip is designed and behavior is simulated using VHDL programming in Xilinx Vivado software and functional logic simulation is done successfully in Modelsim for PCM cell array of sizes (2 x 2, 4 x 4, 64 x 64 and 256 x 256).
- Memory word and bit and word line operation with read and write logic is verified successfully on Virtex 5 FPGA.
- The PCM temperature profile with Finite System Machine (FSM) is simulated in Modelsim.
- The percentage of hardware that is used by the device is given by utilization report of device for the implementation of the chip.
- Hardware of the device used in design implementation includes number of slices of input LUTs, bounded IOBs and gated clocks (GCLKs).
- Timing details provides the information related to combinational delays and maximum frequency. Total memory utilization essential to complete the design is provided.
- The hardware and parameters related to timing increases with the size of cell array. It is obvious that hardware and timing values in chip will increase with cell array size.
- Results of the experimental study of MLC PCM are presented.
- Results of iterative program, pre cycled 1000399 which is greater than 1 million cycles, on a 256×256 cell array is shown.
- Discussion on the impact of endurance cycling and temperature fluctuations on the characteristics of the PCM cells are studied and presented.
- Study the retention of MLC data stored in PCM cell array after subjecting it to multiple read and write cycles is presented.
- Finally, we demonstrate the feasibility of 3 bits/cell storage and retention in PCM through experimental results
- Data related to maximum frequency and combinational delay is provided through timing details.
- Total memory utilization report of completed design is included.

- The proposed work has been tested for over 1 million cycles to test its endurance. Also, the achieved convergence rate is 99.25% signifying betterment compared to previous work.

7.2 Future Work

The memristive phenomenon is old and was reported as an anomaly in research before Chua's postulation in 1971. HP Labs brought paradigm change by presenting a working Pt/TiO_2/Pt memristor. The application range of memristor is immense and has the capacity to touch wide variety of technologies mainly owing to high scalability and unique physical-chemical capability. There are many materials showing memristive effect and can be broadly classified as metal oxides, 2D materials, emerging materials and organics. The commercialization of technology is possible mainly in the areas like ReRAM, synapse, neuromorphic architectures, hybrid circuits, crossbar architectures, deep learning and reconfigurable logic. However, the technology is new and poses many challenges like finding new material which fits into memristive framework, state retention capacity with respect to time, response to read/write stimulus, applications in analog and digital domain, compatibility issues in terms of power requirement and EDA tool which requires complete overhaul.

From PCM perspective the study areas are assessment of computing capacity from memory access and power consumption view point, multilevel memory storage capacity in individual memory cell and formation of new computation algebra/logic, reliability calculations by calculating duration of retention of memory state, improvement in speed of computation, reduction in power consumption, designing and performance evaluation of PCM memory as a product, exploration of new material with better characteristics and performance, robotics, artificial intelligence, neuromorphic hardware, to name a few. Though the technology needs to prove its independent in comparison to the existing technologies in the same domain but memristor presents itself as promising next

generation new technology component, which has the potential to change the way we look at the technology and its applications.

The current thesis work has been extended in form of a book chapter **“Memristive Behavior: Tool for Fault Detection and Repairing Dye Solar Cells”** in the book series “Applied Soft Computing and Embedded System Applications in Solar Energy, CRC Press, Taylor & Francis, **SCOPUS Indexed, Web of Science** and through a paper **“Memristive Metal-Insulator Phase Change Phenomenon”** Phase Transitions, Taylor & Francis, **SCI Indexed.** Both the articles are under review at present.

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APPENDIX – A

Publications

1. Manish H. Bilgaye, Adesh Kumar, Anurag Srivastava, Piyush Dua, "Memristive Phase Change Memory" International Journal of Engineering and Advanced Technology, Vol. 9, Issue 1, 2019, pp (4169-4173). **SCOPUS Indexed**

2. Manish Bilgaye, Adesh Kumar, Anurag Srivastava, Piyush Dua, "Memristor Materials: Working Conditions and Properties" International Journal of Scientific and Technology Research, Vol. 8, Issue 11, 2019. **SCOPUS Indexed**

3. Manish H. Bilgaye, S. K. Nippani, Anurag Srivastava, Piyush Dua "A review of Memristor – Mechanism and Characteristics" International Conference on Advances in Nanomaterials and Devices for Energy and Environment [ICAN-2019], January 27-29, 2019, Paper accepted by the journal Materials Today: Proceedings (Elsevier). **SCOPUS Indexed**

4. Manish Bilgaye, Adesh Kumar, M. Gurunadha Babu, Y. David Solomon Raju "Memristive Behavior: Tool for Fault Detection and Repairing Dye Solar Cells" Book series "Applied Soft Computing and Embedded System Applications in Solar Energy, CRC Press, Taylor & Francis, **SCOPUS Indexed, Web of Science** (Under review)

5. Manish H. Bilgaye, Adesh Kumar "Memristive Metal-Insulator Phase Change Phenomenon" Phase Transitions, Taylor & Francis, **SCI Indexed** (Under review).

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Diploma., Electronic Communication System, Bombay Technical Education Board, Mumbai, 1994

S.S.C., Shirinbai Neterwala School, CBSE, 1990

WORK EXPERIENCE

Quantum University, Roorkee: Sr. Assistant Prof. in Computer Science Engineering Dept. 1/1/2019 to 13/6/2019

Symbiosis Skills and Open University, Pune: Assistant Prof. in Mechatronics Department. 11/8/2017 to 9/3/2018

ITM, Gwalior: Assistant Prof. in Electronics and Communication Engineering. 2/1/2015 to 8/8/2017

University of Petroleum & Energy Studies, Dehradun: Assistant Prof. – Selection Grade in Electrical & Electronics Engineering Department. 11/11/2013 to 31/12/2014.

Prof. Ram Meghe Institute of Technology & Research, Badnera: Assistant Prof. in Electronics and Communication Engineering Department. 2/5/2011 to 8/11/2013

University of Petroleum & Energy Studies, Dehradun: Assistant Prof. – Senior Scale in Electrical & Electronics Engineering Department. 15/6/2009 to 30/4/2011.

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DIMAT, Raipur: Reader in Electronics and Communication Engineering Department. 23/2/2007 to 8/7/2007

Shri Shankaracharya Colege of Engineering and Technology, Bhilai: Senior Lecturer in Department of Electronics and Communication Engineering. 15/6/1999 to 22/2/2007

Declaration:

I hereby declare that the information furnished above is true to the best of my knowlwedge.

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