High Performance ECG Heart Beat Monitoring

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CERTIFICATE

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This is to certify that the thesis on "**High Performance ECG Heart Beat Monitoring**" by **B.KHALEEU REHMAN** in Partial completion of the requirements for the award of the Degree of Doctor of Philosophy (Engineering) is an original work carried out by him under our joint supervision and guidance.

It is certified that the work has not been submitted anywhere else for the award of any other diploma or degree of this or any other University.

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DECLARATION

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which has been accepted for the award of any other degree or diploma of the university or other institute of higher learning, except where due acknowledgment has been made in the text.

B.KHALEELU REHMAN

DEDICATED

TO

PARENTS & MY FAMILY

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

ECG	Electrocardiogram Signal
AED	Automatic External Defibrillator
HRV	Heart Rate Variability
FPGA	Field Programmable Gate Array
FFT	Fast Fourier Transform
HDL	Hardware Description Language
RTL	Register Transfer Level
ISE	Integrated System Environment
MIT-BIH	Massachusetts Institute of Technology, Beth Israel Hospital
ESD	Electrostatic Discharge
AC	Alternating Current
EMG	Electromyogram
EEG	Electroencephalogram
EMI	Electromagnetic Interference
CVD	Cardiovascular diseases
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuit
AWGN	Additive White Gaussian Noise

HRV	Heart Rate Variability
ADC	Analog to Digital Convertor
UART	Universal Asynchronous Receiver Transmitter
S0C	System-on-Chip
UMC	United Microelectronics Corporation
SPHVT	Static Power High Threshold Voltage Process
HVT	High Threshold Voltage Process
DWT	Discrete Wavelet Transform
BLW	Baseline wander
FIR	Finite Impulse Response
IP core	Intellectual Property Core
FSM	Finite State Machine
MWT	Meyer Wavelet Transform
PCA	Principle Component Analysis
LDA	Linear Discrimination Analysis
ICA	Independent Component Analysis
PCB	Printed Circuit Board
ANT	Adaptive Network Technology
AES	Advanced Encryption Standard
HLS	High Level Synthesizer

LLFE	Least Square Linear Phase FIR Filter
LUT	Look Up Table
CLB	Configuration Logic Block
BUFG	Generic Check Buffer
I/O	Input /Output
IOB	Input Output Block
AGC	Automatic Gain Control
FN	False Negative
PPV	Positive Predictive Value
DA	Distributed Arithmetic
SNR	Signal to Noise Ratio
MSE	Mean Square Error
BSN	Body Sensor Networks
LMS	Least Mean Square Algorithm
DOM	Difference Operation Method
LPF	Low Pass Filter
BPF	Band Pass Filter
BSF	Band Stop Filter
IIR	Infinite Impulse Response
PLI	Power Line Interference
RF	Radio Frequency

IF	Intermediate Frequency
IOT	Internet Of Things
CVDs	Cardio Vascular Diseases
IDWT	Inverse Discrete Wavelet Transform
SGSF	Savitzky Golay Smoothing Filter
PPG	Photoplethysmogram
HDL	Hardware Description Language
LAN	Local Area Network
CLB	Configurable Logic Blocks
BPM	Beats per minute
LCD	Liquid Crystal Display
RAM	Random Access memory
ROM	Read Only Memory
STFT	Short Time Fourier Transform
DSP	Digital signal processing
DAC	Digital to Analog Converter
PMOD	Peripheral Module
RA	Right Arm
LA	Left Arm
RL	Right Leg
LL	Left leg

AR	Address Register
DR	Data Register
FIFO	First Input First Output
DFT	Discrete Fourier Transform
DIT	Decimation in Time
DIF	Decimation in Frequency
SIPO	Serial Input and Parallel Output
PISO	Parallel Input and Serial Output
DDS	Direct Digital Synthesis
SPI	Serial Peripheral Interface
LUT	Look Up Table
VHDL	Very High Speed Integrated Circuit Hardware Description Language
XST	Xilinx Synthesis Technology
LED	Light Emitting Diode
VGA	Video Graphics Array
UCF	User Constraints File
STA	Static Timing Analysis
PAR	Placement and Routing
NGC	Native Generic Circuit
NGD	Native Generic Design

JTAG	Joint Test Action Group
USB	Universal Serial Bus
ICON	Integrated Controller
ILA	Integrated Logic Analyzer
VIO	Virtual Input Output
ATC2	Agilent Trace Core 2
IBA	Integrated Bus Analyzer
GUI	Graphical User Interface
FDA	Filter Design Analysis
CS	Chip Select
DSO	Digital Storage Oscilloscope
DUT	Design Under Test
DCM	Digital Clock Manager
LSB	Least Significant Bit
MSB	Most Significant Bit
DV	Data valid
CPLD	Complex programmable logic devices
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
GCLK	Gated Clock
IBUF	Input Buffer

IOBUF	Input Output Buffer
PLD	Programmable Logics devices
VLSI	Very Large Scale of Integration
MSE	Mean Square Error
SSNR	Signal to Signal Pulse Noise Ratio
COR	Correlation Coefficient
SGSF	Savitzky Golay Smoothing Filter

LIST OF ABBREVATIONS

µv	Microvolts
mV	Millivolts
ms	Milliseconds
Hz	Hertz
KHz	Kilo Hertz
MHz	Mega Hertz
W	Watt
mW	Milli Watt
µW	MicroWatts
GHZ	Gega Hertz
nm	Nanometer
mm^2	Square Milli meter
cm	Centimeter
b	Bit
B	Byte
kB	Kilo Byte
MB	Mega Byte
µP	Microprocessor
µC	Microcontroller

EXECUTUVE SUMMARY

Electrocardiography (ECG) is the method of recording the electrical signal of heart by placing the electrodes on human skin. The signal conditioning challenges inherent in this application are primarily due to the small signal of only 0.2 mV to 2 mV peak-to-peak, the 0.05 Hz to 150 Hz bandwidth, and the 50 Hz/60 Hz interference. The analysis of the ECG has been extensively used for identifying many cardiac diseases. FPGA based ECG machine design has low power consumption, delay and higher system performance based medical equipment in medical electronics. In the research work, the high performance ECG system chip is designed and synthesized on Virtex -5 FPGA and real time validation is carried for patient heart beat detection. The research work is categorized in 8 chapters which is summarized below.

Chapter-1 detailed about the introduction to ECG, problem statement, research objectives, motivation and need and thesis organization. The main objective of the research work are summarized as

- Chip design and simulation of real time QRS complex detection algorithm for the ECG signal to calculate heartbeat.
- Perform time domain, noise filtering and FFT analysis for optimal design. FPGA synthesis and validation of developed system.
- Comparison of system performance in MATLAB and HDL environment.

Chapter-2 detailed the research work done in the field by different researches and their outcome. Based on the interferences and literature carried out several researches the high speed ECG signal, processing based system design has the opened platform in the following fields.

- Modeling, design of the several modules of ECG processing system with simulation of real time QRS complex detection algorithm and ‘R’ peak detection for the ECG signal to calculate heartbeat.

- Perform time domain analysis to process the large-scale ECG signal, noise filtering and FFT analysis for optimal design to estimate the optimal hardware resources and timing resources on high end FPGA by optimal code design technique, filter structure and memory optimization techniques.
- Use of the higher end FPGA for the synthesis and validation of developed System to estimate minimum utilization of FPGA parameters.

Chapter -3 detailed the ECG system block diagram and its different components used to explain the top level schematic. The detailed description of all the modules as 3 lead ECG electrodes, Analog to digital converter (ADC) module, ADC interface module, 50 Hz noise removal filter, high frequency noise removal filter, dual port RAM, Short Time Fourier Transform (STFT), magnitude and phase calculation unit , chip scope analyzer /ECG signal analysis unit and digital to analog (DAC) module is summarized. The FFT architecture and ping –pong architecture of 1024 point FFT computations. Chipscope Pro - analyzer as Digital Synthesis (DDS) provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation instead of using function generators.

Chapter - 4 detailed the design methodology ECG chip simulation, synthesis and description of different software tools. There are two approaches in ECG system chip design one is bottom up design another is top-down approach. In the bottom up technique the design is developed for small modules and structured in a top design using structural style of modeling. In this design specifications are considered such as 12 bit ADC, 50 Hz noise removal filter 0.05 to 100 Hz, dual port RAM 32 KB and 1024 points FFT etc. The FPGA synthesis flow has Initial design entry in VHDL, behavioral simulation, Technology mapping, placement ,routing and bit file generation and configuration in Virtex-5 FPGA.

Chapter -5 detailed MATLAB Filter Design Analysis (FDA) tools for notch filer, band pass filter as FIR equiripple filter design. The band pass filter with the

following specifications are used to remove the high frequency noise. The sampling frequency is set to 220 Hz stop band filter of Fstop1 is chosen, as 0.01Hz the pass band filter frequency of Fpass1 is 0.05 Hz and Fpass2 is 100 Hz. The stop band filter Fstop2 is greater than 100 Hz, Fstop2 is set as 101 Hz. The FIR filter is used for the Band Pass Filter (BPF). The BPF allows the lower frequency being 0.05 HZ and the higher frequency being 100 Hz, the band of frequencies The FIR filer coefficients are generated by band pass filter using the equiripple filter. The FIR filter is used for the Band Pass Filter (BPF) application. The BPF allows the lower frequency being 0.05 HZ and the higher frequency being 100 Hz, the band of frequencies. The 30 patient's ECG samples are taken from physionet.org website and the R-peak detection technique is executed with 'z' test statistical technique.

Chapter -6 detailed simulation and design outcomes as main results with respect to designed ADC module, high frequency noise removal FIR filter module, ECG-ROM module, FFT module as STFT, magnitude calculation module and top-level ECG System chip. The hardware design summary and timing parameters are also discussed with Virtex 5, synthesis process, analysis and verification in Xilinx 14.2 ISE and Modelsim software. The ECG data thus obtained from the ROM is sent for FFT analysis of the ECG signal. The 1024-point FFT is calculated for the ECG signal. The number of channels to observe the output on the chip scope or else in the Digital Storage Oscilloscope is set as logical high '1'. The hardware target frequency is 50 MHz. The radix-2 decimation in frequency algorithm is used. The output of the FFT is considered as the fixed-point representation with input data being 12 bit X_n real is the 12 bit input data. X_n imaginary value is set to zero since in the input ECG signal has only real values. The output of FFT has real values and imaginary values.23 bits of data correspond to the real values and 23 bits of data corresponds to imaginary values. The unscaled FFT uses 23-bit output data bits and allows adjacent block RAM with less number of multipliers used. The FFT values are stored in the look up table of the device using 3-multiplier structure for the resource optimization technique all the complex multiplications uses the three real

multiplications and five add or subtract operations. The description of the all pins and functional Modelsim simulation is detailed in chapter.

Chapter-7 details the Virtex 5 FPGA synthesis environment, FPGA synthesis process, experiment setup and chip scope analyzer for real time signal processing in FPGA. The QRS detection and R peak detection from the synthesized test cases, comparative analysis with respect to hardware and timing utilization report is extracted directly from Xilinx ISE 14.2. The value of minimum period is 16.915 ns, 9.312 ns and 8.100 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. In the same way the values of min time before clock signal is 16.452 ns, 9.094 ns and 7.128 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. Maximum time after clock signal is 11.930 ns, 7.804 ns and 6.518 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. The combinational path delay is 7.846 ns, 4.330 ns and 3.592 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. The timing results for Virtex-5 FPGA are optimized in comparison to SPARTAN -3E and SPARTAN-6 FPGA. The value of maximum frequency support is 359.120 MHz, 507.389 MHz and 714.462 MHz for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. The comparative analysis of the existing work with our work revels that the hardware parameters utilization of our work is less in comparison to the work done by Jatmiko et al (2011), D.Panigraphy et al (2015), M.G Egila et al (2016), T.H. Lu et al (2016) and M.A Kumar et al (2018). The No. of slices, No. of slice LUTs, No. of Fully used LUTs, FF pairs, No. of Bounded IoBs and No. of BUFGs on Virtex-5 are 512, 450, 293, 23 and 4 respectively. The results are optimal in terms of hardware parameters synthesized on FPGA. The real time validation of patient heart beat monitoring is done on LCD on same FPGA.

Chapter -8 concluded that Virtex 5 FPGA gives the optimal solution in terms of hardware, memory and timing parameters. MIT – BIH is carried on FPGA based high performance ECG chip system to analyze the heart beat and estimation of the

system accuracy using ‘Z’ test. The FPGA based running in HDL environment are more accurate and faster in comparison to MATLAB simulated environment. The research work will be helpful of MEMS device chip integration for real time clinical applications and wearable embedded systems.

ABSTRACT

The electrocardiogram (ECG) technology has been proved one of the significant method in clinical cardiovascular domain to detect the diseases related to heart and monitoring the electrical activates of the heart. The primary use of the ECG is to detect several cardiovascular diseases that are caused by numerous cardiac arrhythmia such as cardiomyopathy, myocardial infarction, and myocarditis. In the recent time the research is going on automatic heart beat detection, wireless patient's information transformation, ubiquitous computing with IoT and MEMS based chip design and integration. It is possible by the personalized heartbeat classification of a patient and accumulation of medical data with the integration of high performance computing devices. In this research work, the high performance ECG system chip design and performance verification is proposed on higher end Virtex-5 FPGA. The block level ECG system is consist of ECG electrodes, Analog to digital converter (ADC) module, ADC interface module, 50 Hz noise removal filter, high frequency noise removal filter, dual port RAM, Short Time Fourier Transform (STFT), magnitude and phase calculation unit , chip scope analyzer/ECG signal analysis unit and digital to analog (DAC) module. The individual module is design and integrated as structured chip in Hardware Description Language (HDL) environment. VHDL programming language is used to design the code in Xilinx ISE 14.2 software and functional simulation in Modelsim 10.0 software. The code is optimized with the adoption of filter using Filter design tool (FDA) in MATLAB simulation environment. The Virtex-5 (XC5VLX110T) FPGA is used to configure the design and synthesis. The design is verified for different test cases and patient data available on physionet.org (MIT-BIH) for 30 patients. The ECG system is simulated in MATLAB – FDA environment and system error of 0.696 is estimated. The chip design and FPGA synthesis estimated error 0.378 which are acceptable under 'z' test statistical approach for system design. The system performance is analyzed with hardware design parameters such as number of slices, flip-flops, LUTs, DSP elements, IoBs

and memory. In the same way, the timing and delay parameters are analyzed such as maximum frequency support, minimum period, minimum and maximum time before and after clock signal and total delay to check the behavior of FPGA. It is estimated that the developed design has optimized less hardware and timing parameters on Virtex -5 FPGA in comparison ti SPARTAN- 3E and SPARTN 6 FPGA. The comparison of our design is also carried with exiting work. It is estimated that proposed design has optimal hardware solution. The maximum support frequency of the design is 714. 461 MHz that guarantees the higher system performance. The build IP Core of 1024 point FFT make the computations fast and corresponding data is stored in dual port RAM. The real time FPGA signal is analyzed using Xilinx Chipscope pro-analyzer. The real time signal processing and chip verification is carried to monitor the patient heartbeat on LCD display on same FPGA. The biggest advantage of the research work is that it make the system fast, scalable and supports parallel processing on higher end FPGA. The research work will be beneficial for the industries, researchers who are doing work on higher throughput FPGA based ECG system integration, MEMS devices, and IoT based real time embedded solutions.

CHAPTER 1
INTRODUCTION

The chapter details the introduction to ECG system, problem statement, research objectives, motivation and need. The structure of the thesis is also discussed in the end of the chapter.

1. Introduction to ECG

The present cardiovascular diseases have turned into a risk to human life and health for major diseases and number of deaths are increasing year by year. Therefore, center around the expectation of cardiovascular illness finding and counteractive action is a critical importance. An electrocardiogram (ECG) [1, 2, 3] is the estimation and realistic portrayal, regarding period of the electrical signs related with the heart muscles. The application of an ECG is to observe human's heart rate and find the particular heart situations. The fundamentals of ECG estimation are the same for all related areas, but the intelligent elements and necessities for electrical signals fluctuate significantly. ECG measurement devices have very huge machinery to portable devices, which cost around 20,000 Rs to 3 lakh Rs. Now a day, the entire ECG signal comes in a portable Automatic External Defibrillator (AED).

All ECGs devices [7, 9] are used to observe heart rate through cathodes connected to particular areas of the body. The generated heart signals will have an amplitude of few microvolts (μv) to millivolts (mV). The specific use of the electrodes is to enable the heart's electrical movement to be seen from various edges. It displays as channel on the ECG printout. The differential voltage level is presented between two electrodes by individual channel. It is also presented as the differential voltage

between one electrode and the average voltage from altered electrodes. These channels are called leads, or wires. Different ECG systems are available in market such as 12 lead ECG with 12 different channels, 10 lead ECG with 10 different channel, 3-leads [12, 15] with 3 electrodes, 5-leads with 5 electrodes, 6-leads with 6 electrodes.

A regular ECG follows typical pulse or heart cycle, combination of a P wave interval, QRS complex [18, 19, and 20] interval and T wave interval. The U wave in the ECG typically noticeable in 50 to 75% of ECGs. The reference voltage of the ECG is also known as isoelectric line. One ECG cycle wave, which starts from 'P' part of the ECG signal and ends to 'T' part of the signal, sometimes to the 'U' part of the ECG signal. The electrical action of the heart can be recorded at the surface of the body by using an ECG machine [23, 24]. Therefore, ECG is just a voltmeter that uses 12 different leads or terminals to set on different regions of the body.

The QRS complex [25, 32, 35] is the most discriminative highlights of the ECG waveform as it conveys useful information regarding cardiac arrhythmia [2, 37] acute conduction abnormalities, myocardial infarctions, and other heart related diseases. The extraction of the important information of the ECG signal i.e., QRS complex requires advanced signal processing techniques. Preprocessing [26] includes signal filtering in the ECG for undesirable waves and sources of noise. The ECG is used to decide the heart rate by estimating the time between two sequential QRS waves. The heart rate calculation is important since it is possible to find the heart rate variability (HRV). The HRV [37, 59] is having a great importance in clinical activity. The healthy person of the periodic variation in the heart rate, which correlates the breathing. The HRV is examined by the increasing of vagal stimulation to the sinoatrial node during inhale and decreasing stimulation during exhale. The decreased HRV used for clinical marker reduced vagal activities, further HRV is used to predict the sudden heart attack in patients with

myocardial infarction. The ECG signal characteristics is shown in the below fig. 1.1.

The ECG signal is a periodic signal, which lasts for 0.9 seconds, in which x- axis presents the time (t) in milliseconds (ms) and y-axis has voltage in millivolts (mV). The cycle ECG waveform [33, 35] comprises of P, Q, R, S, T and U wave periods. The standard normal voltages values and its duration of P, Q, R, S and T are shown in the table 1.1.

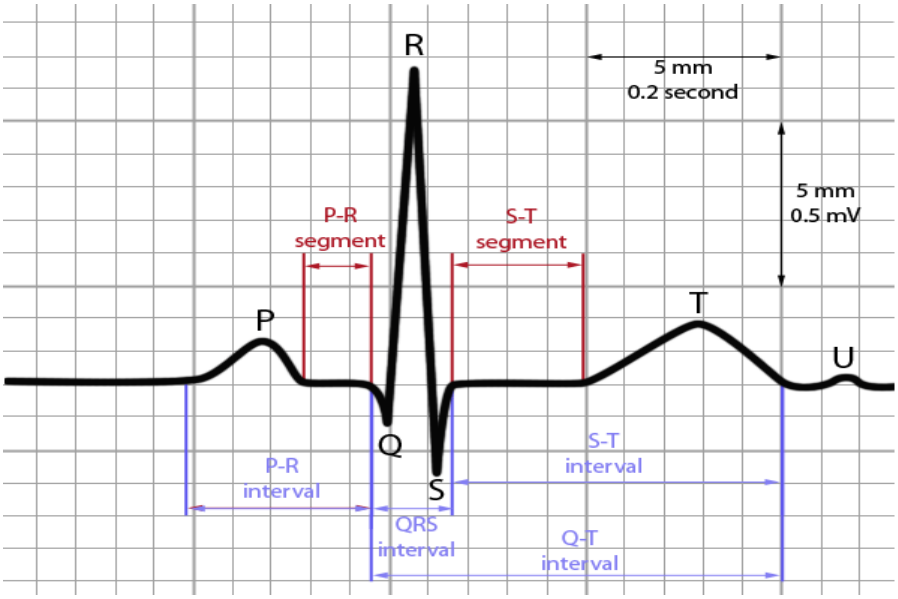

Fig. 1.1. ECG signal characteristics [1, 51]

Table 1.1 Standard ECG data [64]

Amplitude		**Description**	
P-wave	Voltage, 0.25 mV	P-R interval	Time (0.12 to 0.20) Sec
R-wave	Voltage, 1.60mV	Q-T interval	Time (0.35 to 0.44) Sec
Q-wave	Voltage, 25% of R wave	S-T segment	Time (0.05 to 0.15) Sec
T-wave	Voltage, 0.1 to 0.5mV	P wave Interval	Time (0.11) sec
		QRS complex	Time (0.09) Sec
		PR segment	Time (0.06 to 0.10) Sec
		ST segment	Time (0.10 to 0.15) sec
		T wave	Depends on time variation

The ‘P’ wave represents the atrial depolarization. The ‘PR’ interval is the distance between ‘P’ wave and the starting of QRS complex signal. The ‘PR’ interval determines the impulse conduction from the atria to the ventricles is normal or abnormal. The QRS complex wave signifies depolarization activation of the ventricles. The ‘ST’ segment represents the interval between ventricles depolarization and repolarizations ‘R’ wave signifies the ventricle repolarization. ‘QT’ interval is the beginning of QRS complex signal to the completion of the ‘T’ wave. The ‘RR’ interval signifies that one cardiac cycle [53] is completed.

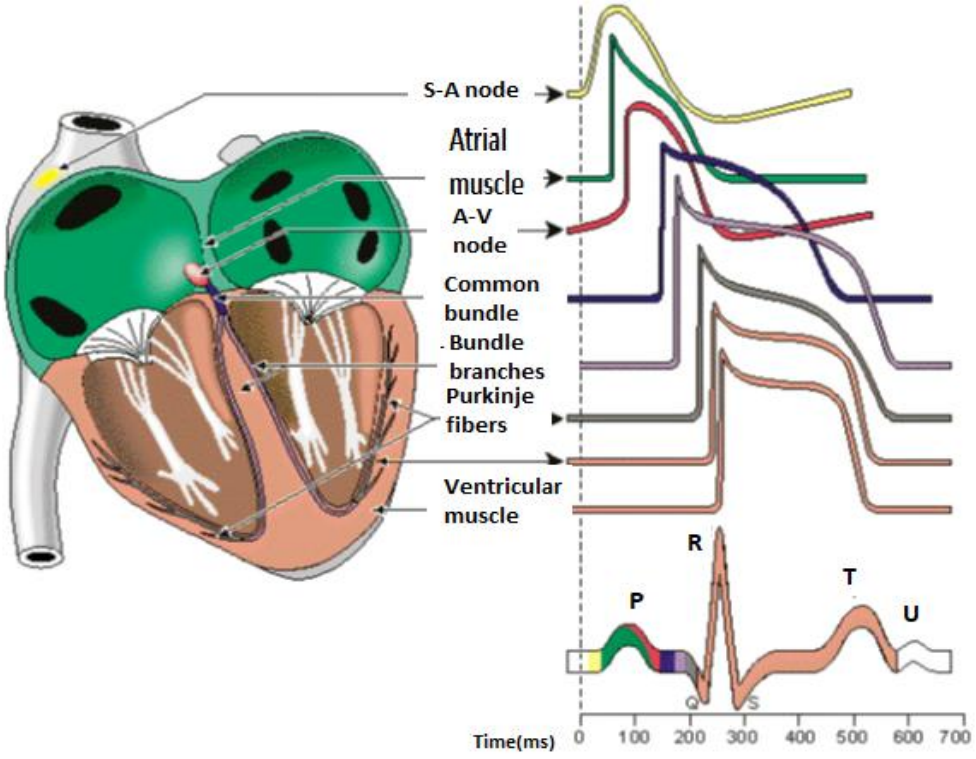

Fig. 1.2 Electrophysiology of heart [53]

The fig 1.2 presents the electrophysiology of heart [54. 58] and its related different functional units as depolarization and repolarization. The resting heart is polarized when the balancing of charge is through out in every cell inside the heart muscle. A cell consist of negative charges as a stimulus. When the positive ions enter in cell, the polarity of the charges is stimulated by changing the charge to positive,

referred as depolarization and happens in individual cell of the heart muscle. This behavior reduces the fiber length, creates the problem for heart muscle and related fibers to be contract on regular basis. The positive particles leave outer part of cell, and reshape its actual size, along these lines relaxing the heart muscle. In this way, the cells are returning to a resting position or polarized state, referred as repolarization. The substance is helpful for building up the body, allows the potential change, happening during depolarization and repolarization to be transmitted and expected at the contacted skin surface. In medical electronics, the ECG has several advantages.

- To check the behavior of heart as electrical functional or not.
- To discover the cause for inexplicable chest torment may be due to the heart assault and irritation of the sac surrounding the heart or angina.
- To discover the cause for side effects of coronary disorder. It may be due to shortness of breath, fainting, dizziness, or sudden change in sporadic heartbeats (palpitations).
- To check whether the barriers of the heart chambers are too thick as upper and lower chambers (hypertrophied).
- To check whether medicines are working and preventing the reactions causing the side effects to the heart
- To check how proper mechanical gadgets are inserted inside heart as pacemakers are employed to control the functionality of an ordinary pulse.
- To check the capability of the heart under different conditions and illnesses such as cigarette smoking, hypertension, diabetes, elevated cholesterol, or a family genetic of early coronary illness.

1.2 Problem Statement

Design and FPGA implementation of high performance ECG system chip to analyze waveform parameters P, Q, R, S and T values for ECG signal analysis and patient's heart beat detection. The synthesized ECG chip will be used for heart beat detection and having features as noise removal system, minimal hardware resources

in the low power, minimum delay. The system can be fabricated as a standalone hardware system or embedded/integrated on a portable electronic devices such as smart phones, smart watches for monitoring patient's heart conditions on a daily basis conveniently. The solutions of the ECG signal are only available in the form of costly instruments. Personal health care equipment needs low cost solutions in the wearable technology.

The problem statement of the research work is given as

"Hardware Chip Design and FPGA Implementation of High Performance Electrocardiogram System for Heart Beat Monitoring Application"

1.3 Objectives

The main objectives of the research work are given below

- Chip design and simulation of real time QRS complex detection algorithm for the ECG signal to calculate heartbeat.
- Perform time domain, noise filtering and FFT analysis for optimal design.
- FPGA synthesis and validation of developed system.
- Comparison of system performance in MATLAB and HDL environment.

The chip design includes the RTL design and function simulation with the estimation of hardware and timing parameters. The software will be used Xilinx ISE 14.2 for the design and FPGA synthesis and Modelsim 10.1b software to check the functionally of the developed design with different test cases. The patient reference data is taken from MIT-BIH database physio net (www.physionet.org), a standard organization [38] to maintain the ECG data and permits to carry out research in medical applications

1.4 Motivation and Need

The well proficient, pharmaceutical specialist, electro physiologist, cardiologist, and anesthesiologist generally do an electrocardiogram (EKG) or ECG [62]. One can get an EKG as a major aspect of a physical examination at the wellbeing family

physician or during a progression of tests at a hospital or clinic. The EKG hardware is regularly versatile, so the test should be possible anywhere. In case of hospitalization, heart might be consistently observed by an EKG system. This procedure is called telemetry. During ECG process, the area on the arms, legs, and chest where little metal circles or anodes are cleaned and might be shaved to give a spotless, smooth surface to connect the ECG lead wires. The special ECG gel or small pads dipped in alcohol might be set between the lead wires and the skin to enhance conduction of the electrical motivations. The 12-leads are connected to the skin on each arm and leg and on your chest. These are connected to an ECG machine that follows the heart action onto a paper. If the older ECG machine is utilized, the leads are moving on various locations of a chest to find the heart's electrical action.

In present time, 3-Lead ECG system are adopted by medical industries. The vectors between two dipole as point charges present the electrical movement. The position of the electrodes on the body decides the angle of the vector with respect to time. Fig. 1.3 depicts the most common type of the electrode placement, referred as Einthoven's triangle [8]. The hypothetical triangle is considered around the heart. The triangle represents blood movement towards heart during each peak, and associates electrically around the limbs. Lead 1 in the ECG wires represents and measures the difference potentials between right arm and left arm. Lead 2, presents potential difference between the left arm and right arm and lead 3 represents the left leg and left arm. Moreover, Einthoven's law details that triangle points can be estimated along their values from one to another known points. It is very important and crucial for designing point of view. It can minimize the whole system design and reduces the complexity of hardware components used. The main important feature is that only two differential amplifiers are required. In the three lead ECG system, two lead are utilized for front-end hardware solutions and third lead is directly associated with software for simple subtraction or addition of values

achieved from the two leads in the analog front end. Fig. 1.4 presents the position of leads as Einthoven's triangle corresponding to right arm and left arm.

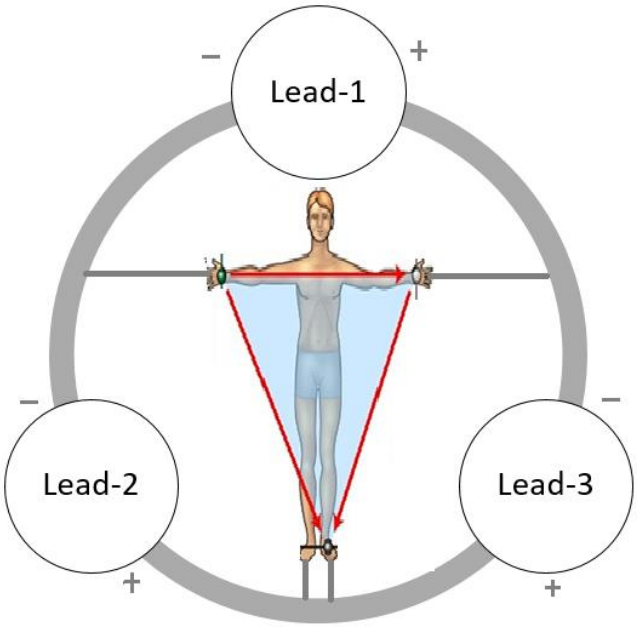

Fig. 1.3 ECG System with, 3 leads ECG

The following equations supports the functionality of the system

Lead 1: $V_1 = \beta_L - \beta_R$ (1.1)

Where, β_L is the electric potential towards left arm

Lead 2: $V_{II} = \beta_F - \beta_R$ (1.2)

Where, β_R is the electric potential towards right arm

Lead 3: $V_{III} = \beta_F - \beta_L$ (1.3)

Where, β_F is the electric potential towards left foot

The analysis of the results shows

$$\text{Lead 1 + Lead 2} = \beta_L - \beta_R + \beta_F - \beta_L = \beta_F - \beta_R = \text{Lead II} \quad (1.4)$$

Similarly,

$$\text{Lead II - Lead I= Lead III} \quad (1.5)$$

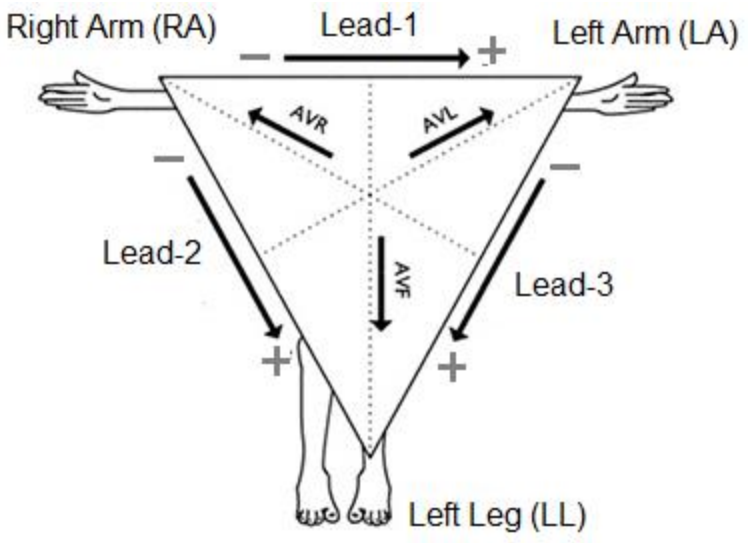

Fig. 1.4 Einthoven's triangle

The ECG is a very safe test. The ECG leads are utilized to exchange a picture of the electrical action of the heart to trace on a paper. In the process, no electricity goes inside human's body from the machine, and there is no risk of getting an electrical shock. ECG signals are consequently vulnerable to several noises. The noise sources can be categorized into three different groups

- Originated noise from external sources to the patient
- Noise originated from the patient in case of moving condition.
- Unwanted electric voltages and interference created due to contacting the patient electrode.

At the point when an energized body is conveyed near an uncharged one, an equivalent and inverse charge is created over uncharged parts of body. For instance, if an ungrounded body is near any electronic machine, associated with 220V, 50 Hz mains supply, the body will build up surface electrons of equivalent and inverse potential despite the fact that minimum amount of current is flowing between the two bodies. This phenomenon is referred as Electrostatic Discharge (ESD). The process of electron exchange because of two objects approaching each other and after that separating by each is known as 'triboelectric charging'. The actuated

potential will have the same frequency similar to main supply, as the frequency of main is 50 Hz.

The noise that occurs in the region of wires carrying AC currents because of the production of the magnetic field by the current flow in all conductors associated with main supply are encompassed by electromagnetic inducted fields. The official website of government of India [5] says the fluctuation in the power supply in India as uninterrupted power supply. As a standard, the main supply power frequency is considered of 50 Hz. The 50 Hz mains supply noise is distinction in voltage, with respect to ground, that is superimposed upon any patient in vicinity to the wire carrying main ac supply current. The patient is driven against the potential that is neither grounded, nor lying somewhere in between of ac mains. The behavior of mains current is always fluctuating. That's what the induced voltage is also subjected to fluctuate to limit the electromagnetic field. Electromagnetic field produced by these live wires is to a substantial degree negated out by the neutral wire adjoining the live wire in the opposite direction.

An Electromyogram (EMG) measures the electrical movement of muscles at rest position and during their contraction. The functionality of EMG depends on frequency. The EEG and ECG both exist in a similar frequency band. The size of EMG wave is five times larger (up to 30mV) than that of the ECG wave in terms of amplitude. Muscular activity can prompt substantial interference in the ECG signal because the ECG and EMG occupy the same frequency band. The ECG wires do not progress as passive non-intrusive conductor. The assignment of any metal adjoining an electrolytic organization as gel over ECG pads is joined with the surface of skin, yields an electrochemical arrangement of half-cell. It is significantly less unpredictable than that of a battery, brings possibilities on the upper surface of the skin. The associated electronic circuit is differential amplifier with a couple of such electrodes used to amplify any distinction in potentials values. The output will be zero, if the cells are identical to each other. If the electric

potential are different, then the potential difference between the two electrodes is considered and amplified further. In this case, small amount of current is delivered by the balanced potential, may cause polarization. Polarization of the electrode will additionally distort the signal. The ECG signal bandwidth [83, 84] is the crucial part in the entire design. The bandwidth of the ECG directs key implementation aspects such as filter bandwidths and sampling rates. Xilinx FPGAs are the best solutions and used by industries for noise removal of ECG signal. Altera FPGA is also an option for noise removal or denoising applications of ECG signal.

Many researchers have addressed the issues on minimum bandwidth requirements for storing and recording of Pediatric Electrocardiograms, [81]. They have applied the same concept on 600 children and investigated the most maximum frequency components available in ECG signal. The research was done by considering the raw ECG signal through serval types of filters, with different bandwidths considerations and employed with sampling frequency of 1.5 KHz, then simulated is carried out in MATLAB environment. The consequences of study demonstrated that in 95% of cases uses 150 Hz filter bandwidth is used as a maximum frequency in case of kids. However, the ideal filter bandwidth is chosen to be 250 Hz in which the filter bandwidth signifies the low pass filter having cut off frequency. Most of the researchers have carried work on high pass noise removal filter [81] i.e. 150 Hz in infants (kids) and 100 Hz in case of the adults. However, more research is going in the direction of low frequency noise removal [86]. The low frequency components in the ECG signal is considered at 0.5 Hz. Sports persons and athletics commonly have low heart rates than the normal heart rate of individual person. The calculation is helpful to check whether 0.5 Hz lower frequency components are available in ECG or not in case of the athletic person. Normally the athletes will have a slower heart rate [2] called as bradycardia. The average heart rate for them is 35 to 60 beats per minute (BPM). The athlete have a heart rate of 35 beats/minute then the frequency corresponds is given as

$$\frac{35 beats/minute}{60\ seconds\ /minute} = \frac{35 beats}{60\ seconds} = 0.58\ \text{Hz} \qquad (1.6)$$

The above equation suggest that the ECG signal should have frequency less than 1 Hz. Apart from the band pass, filter the power line interference i.e. 50/60 Hz noise components and its harmonics removal. The noise can be recognized since the AC supply voltage in the ECG will have the standard frequency of 50 Hz. The most widely recognized reason for 50 Hz interference is the disconnected ECG lead, which yields very powerful disturbing signal and hence required faster response. The Electromagnetic Interference (EMI) from the electrical cables additionally brings poor quality tracings. Some widely used electrical systems such as air conditioner, cooling system and X-rays units have the requirement of heavy electrical cable current. It can induce 50 Hz signals in the input side electrical circuit of the ECG machine. Electrical power system additionally induce to a spike on the wave or rapid pulse. So, it is required to filter out the two noise sources from the ECG signal for precise detection. Analog filter design is also helpful to reduce the problems but it may additionally introduce the skewing of the signal. The non-linear phase shift of the instrumentation also depends on temperature and resistance, which may affects the system performance. The digital technological advancements and new filter design concepts provides system capability and offers more advantages than analog filters in terms of minimum delay, less area, low power consumption and higher throughput.

In a nation, where medicinal services is continually under the spotlight. It is appeared glaringly evident to approve if a special advertise is available in Indian medicinal services for a portable ECG device. The healthcare system in India provides the medical benefits for the large number of population. The budgetary allocation of Rs 52,800 crore for health in 2018/19 was merely 5 per cent higher than the revised estimate of Rs 50,079.6 crore, in 2017/18.[14, 64] Roughly 17% of the total government budget. People in the rural zones find very challenging to travel the cities and the surrounding areas of the city. In a current endeavor to influence health care to mind, more open to the underprivileged the health care department has fixed to keep the mobile health clinics. The health care government

officials ordered the existing hospitals and rural clinics, which do not maintain the medical standards. Such hospitals have the requirements of low cost and flexible ECG machine to fulfil the key necessities for patients and provide sufficient and exact support to people utilizing the device. This ECG device additionally discovers potential use in the private medicinal services division and General Practitioners. ECG test reports tells to their clients and patients for early recognition of conceivable heart conditions. Private attendants who give medicinal care to patients in their homes may likewise utilize the device. The system design with low cost, less area, less power consumption and less delay is the key requirement for both patient and doctor.

ECG wave signifies the electrical exercises of the heart. Each segment of ECG signal has a specific significance, at whatever point any issue causes into the heart the common morphology of the ECG wave has been changed. In the medical treatment, the physician or cardiologist observes him/her will take these changes and the decision. Now an ECG is a non-stationary wave so to check the signal outwardly is not a simple task for a physician and furthermore it is a time consuming procedure. At the point when a patient is in serious condition, requires long time observing. So, it is not feasible for a specialist for long time supervision. So, it is required to automate ECG monitoring system in which ECG wave is taken from the patient's body and eliminates the noises, which occur like the power supply, patient breathing and patient movement noise. Sometimes, it is very difficult for a cardiologist to take the important design by only monitoring it visually due to noises accumulated with the original ECG signal. Therefore, a PC based computerized ECG checking framework is required not just for a grown-up patient. The ECG wave has an awesome significance to know the state of fetal in the maternal midriff. The ECG signal has an extraordinary significance in biomedical science the above information motivates to carry out the research in this field.

1.5 Thesis Outline

The thesis work consists of 8 chapters which expresses the complete thesis. The thesis organization is detailed chapter wise.

- ***Chapter 1:*** The chapter details the introduction to ECG, problem statement, research objectives, motivation and need. The organization of the thesis is also discussed in the end of the chapter.
- ***Chapter 2:*** The chapter discusses the literature survey carried out with the help of different research papers in the field of ECG signal processing, system design and performance analysis. It also focuses on the literature gaps identified and interferences drawn based review.
- ***Chapter 3:*** The chapter describes the ECG system block diagram and its different components used to explain the top level schematic. The chapter also includes the complete description of individual modules, assumptions and modules details to support the functionality of complete system.
- ***Chapter 4:*** The chapter explains the design methodology, different methods, R peak detection, QRS complex detection, filter design techniques. The chapter also discussed the different software tools description form simulation as well as synthesis
- ***Chapter 5:*** The chapter explain the filter design in MATLAB Filter Design Analysis (FDA) tools for notch filer, band pass filter as FIR equiripple filter design. The MATLAB simulation results for ECG signal for different patients is also presented to analysis the R peak detection, and beats per minute
- ***Chapter 6*****:** The chapter details the all simulation and design outcomes as main results with respect to designed ADC module, high frequency noise removal FIR filter module, ECG- ROM module, FFT module as STFT, magnitude calculation module and top-level ECG System chip.
- ***Chapter 7:*** The chapter details the Virtex 5 FPGA synthesis environment, FPGA synthesis process, experiment setup and chip scope analyzer for real time signal processing in FPGA. The chapter also discusses the QRS detection and R peak detection from the synthesized test cases, comparative analysis with

respect to hardware and timing utilization report extracted from FPGA devices. It also compares with the works done by different existing researchers and estimating the comparative system errors on data extracted from 30 patients of MIT-BIH.

- ***Chapter-8:*** The chapter includes the conclusions, drawn from the research work and recommendations about the further research and possibilities.

CHAPTER 2
LITERATURE SURVEY

The chapter details the literature survey carried out in understanding and analysis of ECG signal processing, noise removal, FPGA synthesis with device utilization summary, ASIC based ECG signal processing and implementation techniques in different software . This chapter also discusses the research gaps and findings by different researchers.

2.1 Literature Review

The detailed literature review is given below based on the research work carried by different researchers.

Aboutabikh K. et al [2] proposed all the 4 types of noises associated with ECG signal implemented on the Altera Cyclone II EP2C70F896C6 FPGA. The denoising is carried out by using multiband digital filters. The filtering HDL environment is carried out using the QUARTUS II 9.1 software. A sine is generated and all the types of the filters are carried out like LPF, BPF, BSF using the multiband digital filters and the output is checked on the oscilloscope.

Agarwal, S. et al [4] proposed Savitzky Golay Smoothing Filter (SGSF) implemented on FPGA to diagnose smartly the biomedical signals such as EEG & ECG. The objective of the paper is to remove the noise with very less distortion. The EEG signals and ECG signals are introduced with the noises and such noises are removed and parameters such as Signal to Noise Ration (SNR), Signal to Noise Ration Improvement (SNRI), Signal to Signal Pulse Noise Ratio (SSNR), Correlation Coefficient (COR) and Mean Square Error (MSE). The comparison

table of moving average filter and Savitzky Golay Smoothing Filter (SGSF) is mentioned with respect to device utilization summary and power consumption.

Alhelal D et al [6] described the efficient digital system for the Noise cancellation and QRS complex beats detection in the Electrocardiogram signal. The overall system is implemented in the FPGA. FIR filters are employed for the noise removal and then for the detection of the QRS complex peaks in the Electrocardiogram signal. The FSM chart of the digital system describes about the algorithm of the work the synthesized work is dumped in the ALTERA, DE II FPGA board. The timing and functional simulation work is carried out by using QUARTUS II software. The ECG data input is taken from the standard database for ECG signal i.e MIT-BIH database for the analysis and irregulaties in the heart beat. The ECG samples are taken and then applied the different windowing techniques in windowing stage the adaptive noise and signal thresholding is carried out. The paper presents the hardware accuracy of 98% for the QRS peaks detected and the classification of irregularities in heartbeat is discussed in the real time environment. For noise removal direct form-1 approach is used the FPGA hardware of the FIR filter is used for all the coefficients of the filter are converted into the 8 bit signed numbers. The finite state machine with nine states is discussed where each stage has its own significance like peak detection, thresholding, average RR intervals. The hardware device utilization summary is tabulated with the ALTERA FPGA board.

Azariadi, D et al [8] proposed internet of things (IOT) based ECG signal for the diagnostic purpose of Cardio Vascular Diseases (CVDs) remotely. IOTs based embedded system platform is integrated for the ECG signal analysis and heartbeat. The proposed hardware continuously monitors the ECG signal, which is of small size and comes with inbuilt wearable shirts. DWT is used for the ECG signal analysis and support vector machine is used for the classier. The accuracy of the

overall system is tested and the IOT based hardware is implemented on Intel Galileo board.

Bayasi N. et al [10] integrated ECG system components to detect ventricular arrhythmia by using the Naive Bayes classifier, real time and adaptive techniques are used for the detection of P, QRS, and T waves. The paper compares the validation with the two database one is MIT-BIH database and the second one is American heart association [28]. Based on ASIC simulated results it shows the accuracy of 86% for the sampled data. The system is tested using 65nm CMOS technology. The area of the ASIC is 0.112 square millimeter and power is 2.78 µWatts .The operating frequency of the system is 10kHz.The layout of the design is shown by using the Synopsys tools. The backend tools are used for the implementation of the design.

Bhaskar P.C.et al [13] presented the de-noising of high frequency using Finite Impulse response (FIR) filter using distributed arithmetic approach with Xilinx system generator tool. Instead of using the multipliers in the FIR filter to remove the high frequency, noise the distributed arithmetic (DA) is used. The ECG signal is associated with the muscle noise, after the FIR filter implementation it is subjected to evaluate the signal to noise ratio (SNR) and the mean square error (MSE).The FPGA implemented results are verified by using Xilinx Spartan 3E FPGA board and the MATLAB is used for the analysis and simulation. The standard MIT-BIH database is the standard ECG samples for the input and further processing.

Bucheli. J et al[14] proposed the low-cost system for the measurement of physiological variables. The FPGA based system is used for monitoring blood pressure, body temperature, and graphic heart rate, which will be a tool for physicians and best method for the professionals working in rural areas and utilizing consumer electronics based systems together the patient information and

further processing in serval diseases identification. Experimental results have shown 1% error in the measurement of different variables and standard values

Bhogeshwar S.S. et al [16] proposed the ECG signal de-noising with FIR and IIR filters. A comparative analysis is carried out and SNR is measured. Apart from SNR, accuracy and error is also calculated by using the wavelet tool box. MIT-BIH cardiac arrhythmia database is used for the input to the ECG signal. The comparative analysis shows the better SNR with Butterworth filter having 49.03 and the best accuracy with zero-phase low pass filter with 99.58%

Chabchoub, S. et al [17] proposed a monitoring of biomedical signals based on LABVIEW and FPGA.Bio medical Signals like ECG, EEG, and EMG are monitored for heart, brain and muscle. These signals are extracted then amplified and filtered to observe the output signals on the monitor of a computer screen. Graphic programming for the LABVIEW is used instead of HDL programming.

Chowdhury, S.R. et al [19] proposed FPGA based ECG QRS complex wave detection and then finalizing the tachardia or tachyarrhythmia. The QRS wave is detected using entropy measure of fuzzy logic. To check the algorithms the CSE database ECG samples are used. Hardware is implementation in Altera cyclone EP1C6Q240C8 device. Number of Slices, number used as logic, number used as Input output pins, 5865, 579, and 27 respectively .

Chen W.J et al [21] proposed a lossless low power wearable ECG signal detection device for a long-term diagnostics, which reduces the wireless transmission and replaces the battery. It depends on the run length coding. The coding technique is used to compresses the ECG signal by duplicating the encoded data with the help ECG signal parameters and characteristics. The hardware utilization summary is carried out and the ECG input is taken from the MIT-BIH database.

Chen S.W. et al [22] Proposed the discrete wavelet based ECG signal noise removal and implemented on the FPGA. The preprocessing of the system includes the DWT, thresholding and Inverse Discrete Wavelet Transform (IDWT) modular circuits apart from the thresholding an adaptive thresholding implantation. Synopsys design simulation TSMS 40 nm tool is used for the simulation. The signal to noise ratio is tabulated before noise and after noise.

El Hassan et al [27] proposed FPGA based design and its assessment for a pre-processing phase of ECG signal analysis, which uses discrete wavelet, transform (DWT) and baseline wander noise removal and the QRS complex detection from the ECG signal. The use of the DWT emphasis on the minimal hardware, low power FPGA based device and low cost especially for the portable medical equipment. This paper presents the Xilinx system generation software for the DSP applications and easily plug in with the MATLAB Simulink. The FPGA hardware test is synthesized with standard MIT-BIH cardiac arrthymia database. In the tabulated and simulated data for MIT-BIH database, the baseline wander(BLW) noise is suppressed and noise suppression is observed by hardware software co – simulation. The synthesis was carried to target FPGA chip is Xilinx Spartan 6 on XC6SLX16 device. The MATLAB simulation is also used for finding the FIR filter coefficients and the Xilinx Artix -7 series FPGA board is also used for the implementation and comparing the hardware resources with Spartan 6 FPGA. The discussed base line wander noise is below 0.8 Hz frequency. MALLAT algorithm is used the paper concludes that the optimized hardware is used as IP core for the Xilinx soft core processor.

Egila M.G. et al [28] proposed the FPGA based design for the of ECG signal. This methodology followed high pass FIR filtering technique for the removal of the noise during the processing of ECG signal in FPGA hardware. The device utilization summary on Spartan 3E FPGA kit is discussed. For the de-noising least

square linear filter, technique is used. Discrete wavelet transform is used. The system adopted back propagation based neural network approach to distinguish the sampled values ECG signal. The accuracy of the system is measured and it shows 97.8% for the ECG signal input and the synthesis report for the Xilinx Spartan 3A FPGA hardware is tabulated. The three blocks are involved with Least square Linear Phase FIR Filter (LLFE) design includes noise removal block, feature extraction block and the classifier block. Simulation results are carried out with MATLAB and x-sim to check the functionality behavior and to observe the signal with the noise and the actual signal. The comparative analysis of the device utilization summary is tabulated in table 2.1. The LLFE implemented design on FPGA is carried out with the device Xilinx SPARTAN 3A-DSP XC3SD3400A is compared with the jatmiko et al 2011[51] using the Xilinx Spartan 3A-XC3S700AN.LLFE stands for least square linear phase FIR filter.

Table 2.1 Device utilization report comparison of ref [28] and ref [51]

Logic utilization	LLFE approach (Resources)	Jatmikoet al.(2011) (Resources)
Slice flip flops utilization	3893	7301
4 input LUTs utilization	3953	7654
4 input LUTs utilization	4321	8832
Bounded Input/output blocks utilization	140	14
BUFGMUX utilization	4	4

El-Sayed et al [29] proposed the wireless transmission of ECG signal using the Altera cyclone III FPGA. Hardware utilization summary is tabulated the functional and timing analysis is carried out using the Modelsim simulation.

Fang W.C. et al [30] The complete set up for compact ECG observing, with an system on chip processor for the relation between time domain and frequency domain analysis of Heart Rate Variabilty (HRV) is discussed in this paper. The

primary capacity of framework contains three sections a simple computerized ADC hardware device, a HRV processor, and lossless compression engine. ECG signal information gained from analog front-end circuits through the ADC controller is sent through the HRV processor for further analysis. Next stage will be the HRV processor performs real time analysis of time domain and frequency domain HRV by using the Lomb periodgram and a sliding window technique. The Lomb periodgram is best for spectral analysis of unevenly sampled data and then applied to time and frequency. Analysis of Heart rate variability (HRV). At last the ECG information are compacted by 2.5 times using the lossless compression engine before observing output using UART protocol. Bluetooth technology is used to transmit the HRV information and the ECG information to a remotely location to monitor and further analysis. The incorporated ECG system configuration has been implemented by using UMC 90 nm CMOS technology. The developed ECG SOC uses the 3-lead ECG data and remote monitoring. The ECG System-on-Chip configuration is scheduled for tape-out under UMC 90 nm SPHVT 1.0V 1P9M process. To minimize static power utilization, the chip has been implemented utilizing high threshold voltage process (HVT) library. The total power utilization of chip is 523 µw, which is simulated with Synopsys Prime Power software. CMOS Back end tools are implemented for the processing of the system.

Gaikwad K. M. et al [31] proposed the high frequency noise removal by using the Butterworth digital filter and its realization, The 100 Hz high frequency noise is removed the process of before filtering and after the filtering operation is shown. The comparative analysis of different filters and the signal to noise ratio is discussed. MATLAB simulation tool is used for the proposed system.

Gradl S. et al [32] proposed the heart rate detection algorithm to detect the QRS complex wave from the ECG signal and to find the 'R' value using a threshold voltage. The simulation analysis for 'R' peaks using MATLAB is carried out for the standard MIT-BIH database.

Gu X. et al [34] proposed the wireless a streaming architecture is implemented on FPGA for the real time detection and for the analysis using the pipelining and the parallel method. The association rule mining is incorporated for the generation of early detection of the signal for the better performance data mining algorithm associated with the hardware is used. The proposed system has shown the low cost, good scalability and less hardware solutions for the suggested system.

Hasan A. M. et al [36] proposed the ECG Baseline Wander (BW) noise removal using the MATLAB simulation tool. The technique behind the scheme was to compare the signal with discrete multi rate filter banks. The comparison of multirate and moving average filter is also carried for adaptive filtering. The algorithm is tested on the FPGA and the comparison of the synthesis report is tabulated by comparing the others work.

Islam M.K. et al [49] The analysis of ECG signal by using the MATLAB simulation tool and the processing of the signal like feature extraction, de-noising is discussed. Simulink is used in MATLAB and LabVIEW software based approach. With LabVIEW digital filter designing and advanced digital signal processing tools are used.

Jayant H.K. et al [50] Proposed an effective digital infinite impulse response(IIR) filter of second order to remove the power line interference(PLI).To perform the task minimax optimization technique is used, for the minimization of root mean square error value after the simulation results the validation is performed on FPGA and LabVIEW environment. Signal to noise ratio is calculated.

Kaya D. et al [52] proposed the LAB VIEW based ECG signal analysis and denoising based on discrete wavelet transforms. The results are tested with the different wavelets finally the cardiac arrhythmia is tabulated for different test cases

Karim M. et al [55] proposed the ST segment in the ECG signal to predict the myocardial infraction. STEMI stands for 'ST' segment elevation myocardial fraction. The FPGA processed ECG signal is carried out using the SPARTAN 6-XC6SLX16 device and the softcore processor is developed using the XILINX microblaz.12 lead ECG data is collected from the physionet bank ATM the system provides the accuracy of 99.41% and sensitivity of 62.5%.

Kurakula,S. et al [56] proposed the detection of QRS complex wave in the ECG signal by using the discrete wavelet transforms using quadrature spline wavelet. The system is implemented on the FPGA hardware and the throughput is measured which comes approximately 52.662 M Samples/sec.

Kumar M.A. et al [57] proposed the R peak detection method from the QRS complex of an ECG signal based on snappier execution, basic testability, and confirmation choices are accomplished by the utilization of the FPGA. The first step is the noise removal in the ECG signal through band pass filter and the first order differentiation process. The second step is envelop extraction of stage through which the Shannon's energy and zero phase filtering. The third stage is the peak finding stage through which the Hilbert transform and the moving average filter is carried out and finally the 'R 'peak is detected on Virtex-5 device XC5VLX20T. The device utilization summary is shown in the table 2.2.

Table 2.2 Device utilization on device XC5VLX20T

Logic utilization	**Used**
No. of slice registers	1086
No. of slice LUTs	1408
No. of Fully used LUTs, FF pairs	1052
No. of Bounded IoBs	82
No. of BUFGs	2

Lee W. K. et al [59] presented the smart way of measuring the heart rate variability (HRV) with the help of 3 electrodes fabricated into a patch. The patch performs the signal filtering, Analog to digital converter and the 'R' peaks detection in the ECG signal for long term HRV analysis. 'R' peak detection using the fabricated device is measured and calibrated under various conditions of the patients like mental stressed, patients were tested and the walking speed of a 5 km/hr patient is tested. The results obtained are sensitivity and very less error. To verify the device the standard MIT-BIH database ECG samples are used as an input to the device. The algorithm developed is based on the automatic gain control (AGC) and indigenous threshold of the maximum amplitude.

Liu X. et al [60] proposed the energy efficient and less area ECG signal data acquisition and signal analysis application sensor node for remote body territory systems. These sensor nodes can precisely record and recognize the QRS waves of ECG waveform with high frequency noise removal. The system used Complementary Metal Oxide Semiconductor (CMOS) technology with area being used 0.18µm. Further it has followed two chips, one being analog front end Integrated circuit(IC) and second one being Application Specific Integrated Circuit (ASIC) for specific digital application. Digital ASIC consumes 9 µm at 32KHz with 1.2 square milli meter and then the analog IC consumes 79.6µWatts power and 4.252 square milli meter. This ECG sensor hub is helpful for long haul observing of cardiovascular state of patients and is extremely appropriate for on-body WBAN application [101, 102]. In order to verify the proposed QRS complex [103]wave Scheme the fixed-point notation level, MATLAB simulation is performed. The simulation is processed using ECG information records from MIT-BIH database for the assessment of the calculations. To minimize the noise and to verify the noise removal the Additive White Gaussian Noise (AWGN) is added with signal to noise ratio being 5 dB for the pure original signal. CMOS back end tools are used for the implementation of signal processing.

Liang Y. et al [61] proposed the ECG signal processing and transmitting the ECG signal wireless. Pseudo differential identification is used for noise removal by using the FIR digital filter. Mathematical morphology techniques is used to detect the QRS complex wave.

Luu, L. G et al [64] proposed the wireless data acquisition system and to capture the process the biomedical signal especially ECG signal in the real time environment using the MATLAB. The proposed hardware consists of the inbuilt Wi-Fi with four additional slots for the interfacing of sensors like ECG, EMG and Sensor Probe for Pulse Oximetry (SPO2).

Martis, R.J. et al [69] detailed Discrete Wavelet Transform (DWT) to represent P -QRS-T wave. The ECG signal values are taken form the MIT-BIH cardiac arrhythmia database and then ECG signal de-noise is carried out by using discrete wavelet transforms the noise suppressed signal is subjected to the QRS complex wave detector using the pan and Tompkins algorithm. For one complete cardiac cycle, the 200 samples of QRS wave is detected then the 100 samples on the right and 99 samples in the left.one being the middle is the reference to calculate the heartbeat. The 110,094 beats are detected using the standard ECG database. The DWT is used to filter out the noise using FIR filter and the Meyer Wavelet Transform (MWT). The 3-dimensionality reduction methods, which uses Principle Component Analysis (PCA), Linear Discrimination Analysis (LDA) and Independent Component Analysis (ICA) to reduce the dimensions of DWT coefficients. PCA works on a direct dimensionality decrease system that looks for projection of the information into the directions of highest variability. The comparison of ECG beats using MIT-BIH cardiac arrhythmia database for different researchers is tabulated and its accuracy is checked this paper shows the performance results of accuracy, specificity and sensitivity 99.28%, 99.83% and 97.97% respectively.

Mirania, S. K. et al [70] proposed to minimize the computational cost in the ECG signal processing by using the multirate signal processing as compared with the conventional digital filtering with the MATLAB simulation tool multirate signal processing is used to separate the slow periodic signals in the heart arrhythmia in the real time environment. Down sampling multirate structure is designed to reduce the aliasing and the length of the filter.

Massagram W. et al [71] proposed ASIC based the heart rate variability (HRV) system implantation. HRV calculates the heart rate by using the RR interval and stores the value in the internal memory for the real time. Some long term ECG signals and short term ECG signals are used as inputs from physionet website for testing purpose. ECG signals for the 2 minutes time is captured and heart rate is calculated on the simulated ASIC chip that consumes the dynamic power of 10 µWatts and 500nm CMOS technology backend tools are used with a die size area 3*3 mm^2.

Ngounou M.et al [75] proposed an instrumentation amplifier with the discrete components that removes the low noise that is associated with the ECG signal. An instrumentation amplifier with negative feedback is used for the optimized de-noising of the signal

Nemati, E. et al[76] presented the ECG wearable sensor, can transmit the wireless data using a standard protocol and the sensor is made up of a capacitive sensor for the processing of low power devices and the fast data rate transfer the ANT protocol is used. The Capacitive ECG detecting is a basic strategy that stays away from direct contact with the skin and gives more comfort to the patient. Tiny capacitive electrode were embedded into a T-shirt of cotton type together with a signal processing and transmitting board with a two-layer standard Printed Circuit Board (PCB) technology. This entire system is of low cost, less power apart from the above motion artifacts noises are suppressed and the results are compared with

glued electrode ECG pads. The technician can easily be readable the wireless transmitted ECG data. This paper concludes the wireless ECG data transfer on a PC screen or any other displaying device, for the wireless data transmission the ANT protocol is used.

Nandagopal V. et al [77] proposed the ECG signal processing using the LABVIEW software. The de-noising of baseline wander from the ECG signals is discussed. The computer screen shows the ECG signal in the real time environment. This signal can be sent by using the LAN cable or ethernet cable to doctors for proper diagnostic.

Ojha, D. K., et al [78] proposed the MATLAB based study and analysis of P, QRS, T and U waves and the noise removal in it. Initially the raw ECG data is preprocessed and then abnormal peaks present in the signals are predicted and compared with the normal signals.

Panigrahy D. et al [79] designed and implemented FPGA based entire ECG system The five blocks methodology is used to detect the QRS complex wave and to find the heart rate. The blocks includes addition, multiplication and data conversion like real to the fixed point representation and fixed point representation to the real is carried out. The ECG samples are taken from the 48-channel MIT-BIH database. The positive predictive values shows 99.89% the sensitivity shows 99.94% and the accuracy shows 99.84%.The preprocessing stage for the ECG samples includes the multiplication if the two binary numbers using the booths multiplier algorithm[33]. The input ECG signal is in the analog form i.e., the amplitude of the ECG signal is real value. The real value cannot process in the FPGA. The conversion of real to fixed point or floating point should be carried out. The fixed-point notation is chosen which takes the less area and less processing time. Only ‘R’ peaks are detected in the paper and the rest ECG parameters like P and T are ignored. The timing simulation results are shown using ISIM simulator. The 48 ECG samples

are considered for simulation, sample number 100 is taken from MIT-BIH database. In the database, # 100 and its true positive beats are considered where the 'R' peak is above the threshold i.e., above the zero axis 'FN' stands for false negative and the average is taken for calculating the sensitivity, error rate, accuracy and Positive Predictive Value(PPV). The comparative of the other signal processing methods for detecting 'R' peak is also tabulated. The FPGA hardware usage by using virtex-5 board is shown below in table 2.3.

Table 2.3 Device utilization report of heart rate calculation system [79]

Synthesis summary report			
Logic utilization	**Used**	**Available**	**Utilization**
Utilization of No. of slice registers	5728	607200	0%
Utilization of No. of slice LUTs	88456	303600	29%
Utilization of No. of fully uses LUT-FF pairs	188	93996	0%
Utilization of No. of bounded I/O Blocks	114	700	16%
Utilization BUFG/BUFGCTRLs	1	32	3%

Ravanshad N.et al [82] proposed ECG processing signal processing using a backend tools, CMOS 0.13µm technology is used to detect the 'R' peaks of the ECG signal which consumes a power of 622 nW, area of the ASIC is 0.136 square millimeter, supply voltage is 1.2 V. The raw ECG data is taken from the MIT-BIH database and the accuracy, sensitivity, positive productivity of the system is measured.

Shukla A. et al [86] presented the FPGA based ECG signal processing is presented in the paper. The design is based on the software based to distinguish the QRS complex wave in the ECG signal. This algorithm detects the next cardiac cycle QRS wave. The average of the ECG peaks are considered. The accuracy of the system is showing 96% for the detected peaks using the standard MIT-BIH ECG samples

database. The design is implemented on the Xilinx Spartan 3E FPGA hardware by using the Xilinx system generator software. FIR filtering technique is used for noise removal. The device utilization summary on Spartan -3E FPGA kit is discussed.

Shin W. et al [87] proposed a compact 8- bit microcontroller and digital filtering in the ECG signal, photoplethysmogram (PPG). Integer based algorithm is developed, and ZigBee modem is used for ECG data commination for remotely accessing. The accuracy is checked and compared with other researchers.

Ting-Hsuna LU. et al [91] presented the QRS complex detection using the difference operation method (DOM). MATLAB is used for the simulation and for the analysis after the simulated results it is then processed in the FPGA for the hardware implementation using the Verilog HDL model. The raw ECG data is taken from the MIT-BIH database and the accuracy of the system is measured using the worst case in the database. The hardware device utilization summary is compared with the pan-Tompkins approach and shown in the table 2.4. The different ECG samples are collected from the standard database and the peaks are calculated and analyzed. Spartan 3E FPGA device is used for testing. The synthesis report for the entire signal is extracted from Xilinx software.

Table 2.4 Device utilization chart comparison [91]

Logic utilization	**Difference Operation method**	**Pan-Tompkins method**
No. of slice registers	966	2901
No. of slice LUTs	842	3443
No. of Fully used LUTs, FF pairs	4321	8832
No. of Bounded IoBs	46	56
No. of BUFGs	1	4

Van Helleputte N. et al [92] proposed the multi sensor biomedical IC, which includes the features, integrated Digital signal processor, analog front end with low power and good performance. The bio medical ASIC depends on 180nm technology with 1.2 supply voltage.

Wang L.H et al [93] proposed the wireless data acquisition system by using a System on Chip (SoC) especially the ECG signal monitoring. The proposed system is subdivided into the three parts first the ECG data acquisition second protocol used for ZigBee communication third the RF (Radio frequency) transmitter circuits. The SoC CMOS RF front end which consists of the quadrature voltage controlled oscillator and 2.4GHZ low IF transmitter for the ECG signals to transmit wireless CMOS backend tools are implemented using TSM 0.18 µm.

Wang X. et al [94] proposed the System on chip (SoC) based cloud system for the bulk ECG data analysis for the network input output handling hardware for data processing using the pipeline hardware architecture for parallel processing in a single FPGA. The bulk ECG data is compressed transmission control protocol/Internet protocol hardware stack using a macro pipeline architecture to accelerate network packet processing then the streaming architecture to accelerate signal processing, QRS complex wave detection, feature extraction and classification. The device utilization as slice registers; slice LUTs, BRAM and DSP elements are found 19.0 %, 34.7 %, 31.1 % and 53.1 % on Virtex-5 device XC6VLX550T, with the available resources 687360, 343680, 2528, and 864 respectively.

Wess M. et al [95] proposed the ECG cardiac arrhythmia based on artificial neural network and machine learning algorithm on FPGA, to detect the abnormalities on the ECG signal. It provides great accuracy, system performance in comparison to statistical approach. The principal component analysis technique is used for feature extraction multi-layer perceptron based classification. The hardware utilization

summary, accuracy is checked using fixed point and floating point number representation.

Zhai X. et al [98] suggested inter connected technology, deals with the security gadgets, portable medical devices and communication systems, used to monitor the history of the patient remotely. The patient details and the medical reports should be securely transmitted to the doctors through a connected network for the analysis and further diagnosis. The security features are incorporated in the interconnected health system, which includes the network security algorithms. Advanced Encryption Standard (AES), and ECG system. The ZYNQ series FPGA hardware is implemented and parameters like processing time, hardware usage and the power consumption are tabulated. The ECG processing time is calculated as 10.71 mill seconds, power consumption is 107mw and 30% of the ZYNQ FPGA resources are used. The ECG is processed using the principal component analysis and the multiresolution. The FPGA implemented results are verified with the data obtained from the two ECG sensors and the public domain ECG samples i.e., by using MIT-BIH database. The High Level Synthesizer (HLS) is used to write the coding in C/C++, which converts the synthesizable format, Hardware description language to communicate the FPGA. For the interfacing, and for the communication AXI-lite slave peripheral interface is used which is the part of FPGA.

Zhang C.F. et al [99] presented the VLSI based QRS detection technique with the help of body sensor networks (BSN). The mathematical morphing techniques are used to de-noise the baseline wander and the muscle noise as background noise from the original ECG signal. The low pass filtering technique is employed to amplify the QRS complex signal and to strengthen SNR. The algorithm is tested with the wearable connected devices and with the MIT-BIH database. Area and power calculations are tabulated in the Nano FPGA board. The detection rate of the QRS complex is high and the speed is very high. The comparative chart for the detection of peaks and the detection of the peaks with different researchers is

tabulated. The QRS detection algorithm of the ECG is applied for the walking state, running state and breathy deeply state and its MATLAB simulated waveforms are shown.

Zhou Z. et al [100] detailed about the noise removal technique of the ECG signal using FPGA. Model based design for the ECG signal is developed and de-noising is carried out using the adaptive threshold least mean square algorithm (LMS) on FPGA. The hardware device utilization summary is tabulated. Xilinx system generator software is used with the help of Simulink in the MATLAB for the ECG signal.

2.2 Research Gaps

Different researchers on the ECG signal processing in the field of the simulation of the several block of ECG block diagram, filtering techniques, filter design, and FFT signal processing carry out the literature review. Many researches have reported the work by the synthesis process on FPGA. The common FPGA used in SPARTAN 3E, SPARTN-6, Altera, Cyclone-2, high end Virtex FPGA. The chip design and synthesis is carried on Xilinx ISE, Modelsim and Quarts-II software. N the ECG signal processing the most of the simulation work is carried in MATLAB simulation environment. The band pass and notch filters are used as noise removal filter and real time signaling is also done on DSP processors. The TMS TI TMS320C67 processor is used to process the ECG signal following times based starter kit (DSK). The frequency support of the kit is limited to 200 MHz. Some researchers are working on high end applications but they are limited to the use of FPGA, filter design, and real time solutions.

The research papers have reported the analysis and simulation of ECG signal on FPGA to estimate the hardware utilization on Xilinx devices. The detailed synthesis report for the parameters is also carried to estimate the minimum hardware space. The hardware utilization depends on the parameters such as number of slice flip-

flops, number of input/output blocks, LUTs, memory utilization etc. The literature review reported the work based on the simulation and analysis of ECG signals and the noise removal using MATLAB, simulation of the ECG signal processing using different algorithms, noise removal using different techniques, Simulink based model is design, wavelets [104], multirate signal processing based design, IOT based model by using MATLAB.

The literature review based on CMOS technology back end tools for the ASIC is also discussed. The LabVIEW based simulation environment is also used for ECG signal by the researchers for data acquisition system and the wireless communications based system applications. Wireless ECG signal using ANT protocol is also used for Zigbee based wireless communication and intelligent devices are developed for health monitoring [105]. With the advancement in the technology the FPGA's based design are increasing rapidly and used in the medical applications for its low power consumption. Flexibility for the programmers in the HDL, easily transferable and short development cycle apart from the above advantages the FPGA's digital design is easily converted into the ASICs [97] for the real time processing system. FPGA also include the configurable logic blocks(CLB), logic elements, input outputs and interconnections blocks which is different from the DSP processors and microcontrollers which depends on von Neumann architecture. The best part of the FPGA based system is that FPGA provides the reconfigurable and scalable architecture based on pipelined and parallel processing. The current FPGA provides the platform to synthesize the design on higher frequency with less power consumption, minimum delay and area.

The 'R' peak detection in the ECG signal is a method to diagnose heart rhythm irregularities and also to calculate the heart beat that is Beats per minute(BPM). Existing solutions come up with Microcontroller based systems and low Capacity FPGA like SPARTAN-2, SPARTAN-3 FPGA, which are limited to 180 nm technology and having larger delay. Several algorithms are developed to detect the

QRS complex in the ECG signal d FPGA hardware. The entire ECG signal-processing algorithm is developed on different FPGAs by configuring different filters with less delay, low cost, less area and less power consumption. Still there is lot of scope in the research to optimize the design and validate in real time applications. Based on the interferences and literature carried out several researches the high speed ECG signal, processing based system design has the opened platform in the following fields.

- Modeling, design of the several modules of ECG processing system.
- Simulation of real time QRS complex detection algorithm and 'R' peak detection for the ECG signal to calculate heartbeat.
- Perform time domain analysis to process the large-scale ECG signal, noise filtering and FFT analysis for optimal design.
- Estimate the optimal hardware resources and timing resources on high end FPGA by optimal code design technique, filter structure and memory optimization techniques.
- Use of the higher end FPGA for the synthesis and validation of developed System to estimate minimum utilization of FPGA parameters.
- Statistical methodology can be used over sampled number of patient's to understand the error and performance of the designed system.
- Comparison of system performance in MATLAB and HDL environment and estimate minimum area, delay and higher system performance for future medical electronics applications.

CHAPTER 3
ECG SYSTEM AND SIGNAL PROCESSING

This chapter describes the ECG system block diagram and its different components used to explain the top level schematic. The chapter also includes the complete description of individual modules, assumptions and modules details to support the functionality of complete system.

3.1 ECG System Level Block diagram

The system level block diagram of the ECG signal processing system [65, 66] is shown in fig 3.1. The main parts of the diagram are 3 lead ECG electrodes, Analog to digital converter (ADC) module, ADC interface module, 50 Hz noise removal filter, high frequency noise removal filter, dual port RAM, Short Time Fourier Transform (STFT), magnitude and phase calculation unit , chip scope analyzer /ECG signal analysis unit and digital to analog (DAC) module. The human body consist of the 3 lead ECG electrodes connected in 3 different parts of the body in the position of a triangle. One lead is connected in the right arm, second lead in the left arm and the third lead is connected to the left foot. The data obtained from the ECG leads are the analog values. Hence, it is required to convert the values in digital with the help of ADC module. The ADC interface module will convert the analog signal to the digital signal with the Peripheral Module (PMOD) connector inside the FPGA. The digital data obtained from the ADC is given to the digital filters. The Infinite Impulse Response (IIR) notch digital filter is used to remove the 50 Hz power supply noise.

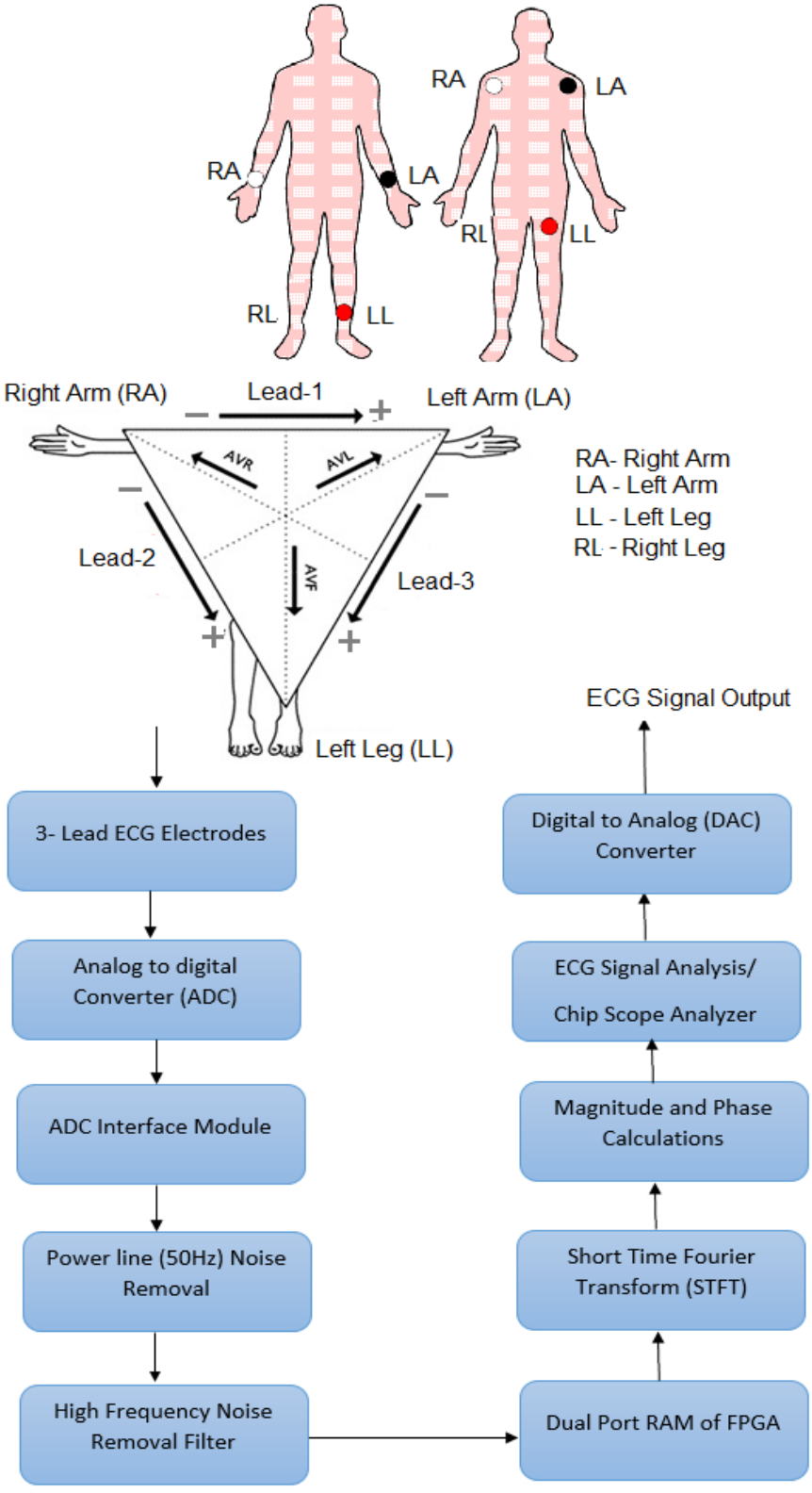

Fig. 3.1 ECG system block description

The data obtained from the Notch filter is sent to high frequency noise removal filter. This filter is designed to attenuate signals, which are not in the frequency range of 0.05 Hz to 100 Hz allowing low pass filter 0.05 Hz and high pass 100 Hz. The output from high frequency noise removal filter is given to dual port RAM of FPGA. The data will be buffered in a dual port RAM. The main operation of the dual port RAM is to write and read the data on input and output ports concurrently. Noise filtered ECG data is written in RAM memory and the same data is read towards another end of RAM and processed for Short Time Fourier Transform (STFT). The main block of STFT is 1024 point FFT on filtered ECG signal to process is fast. STFT is used to analyze frequency response of the heartbeat of human. The obtained values of FFT are given for calculating the magnitude and phase response of the FFT block. The magnitude block will compute the magnitude of the signal from the FFT output. The ECG signal analysis block will display the time domain analysis of the ECG signal (P, Q, R, S and T). The Xilinx Chipscope pro analyzer will display the processed ECG signal in software for analysis purpose. The Chipscope also has the feature that we can analyze the original signal, noisy signal, sampled FFT output. The function of Digital to Analog (DAC) is convert the FPGA digital output to original ECG signal or analog values for real life applications.

3.1.1 ECG Electrodes (3 - leads)

The 3-lead ECG system is widely used technique for measurement of heart rate in the clinics, hospitals and for the continues monitoring of the patients who are suffering from the heart diseases. Most of the 3-lead electrodes comes with the different color coding namely red, yellow and green. The placement of the leads is discussed in fig. 3.2. In the diagram, first lead (red) is connected the right arm, second (yellow) is connected to the left arm and the third lead (green) is connected to the left lower leg towards ankle side. The white, green and red colors are for Right Arm (RA) indication, left Arm (LA) indication, Right Leg (RL) indication

and Left Leg. (LL) indication and respective positions. The measurement is taken across the three lead (RA, LA and LL) or (RA, LA and RL).

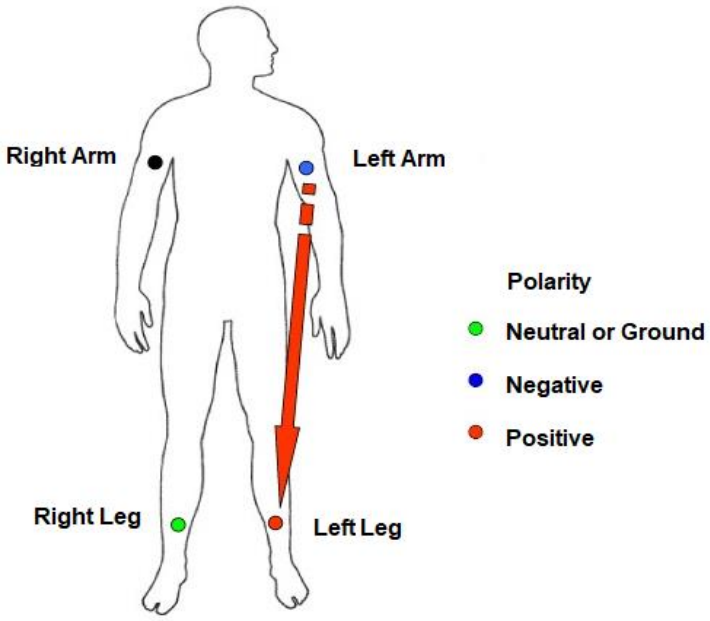

Fig. 3.2 Electrode Position (4 leads can be used as 3-lead ECG)

3.1.2 ADC Module and Interface

The analog input of the ECG is given to ADC, converts the analog input signal to digital signal. The 16 bit ADC is used in which 12 bit are used for the same purpose and four bit are ignored. By making use of the slide switch present in FPGA kit, the real ECG signal or simulated ECG signal can be processed. If the switch is '0' then the ECG simulation analysis is carried out. If the slide switch is '1' then the real time ECG signal is processed. This module converts the analog input that comes from the ECG electrodes and converts into the 12 bits.

The ECG signal has very small amplitude values, which is in the milli volts (mV). The data acquisition system, amplifies the analog ECG, input signals and the amplified values are 0 to 3.3 Volts. The 0 V is the minimum value and 3.3 Volts is the maximum peak value of the ECG input. The 12-bit digital data is of the range of 0 to 4095. Successive approximation type of analog to digital converter is used

where each analog value is converted into the digital with 12 bits of data. The block diagram representation of successive approximation type ADC is depicted in fig. 3.3.

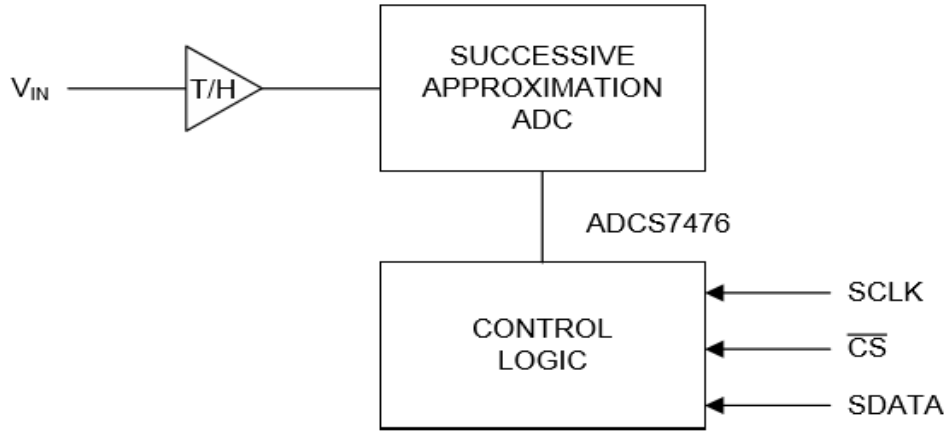

Fig.3.3 Successive approximation ADC block

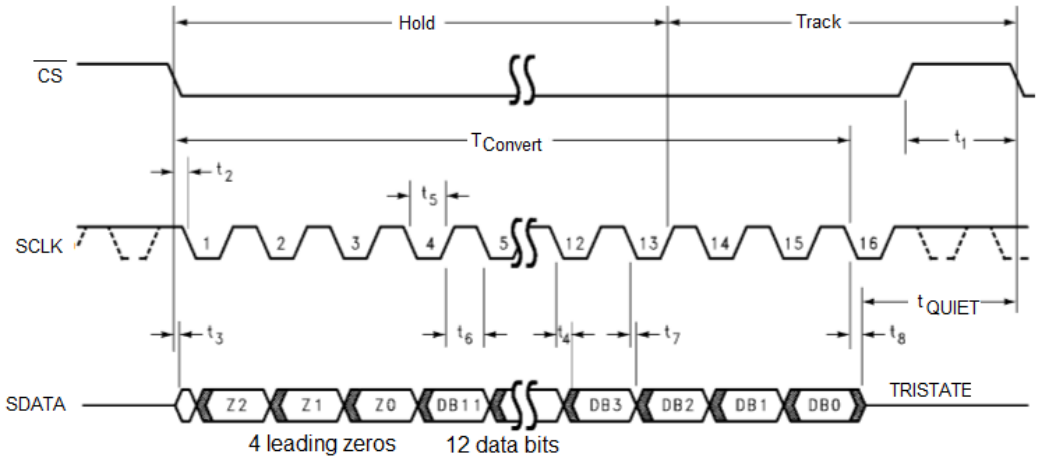

Fig.3.4 Timing diagram for 12 bit ADC

FPGA supports the inbuilt Peripheral Module Interface (PMOD) converts the serial data to parallel data by writing the appropriate HDL code for example the value of 'P' wave in the ECG signal which 0.0025 is converted into the 12 bit binary number using the floating point representation of the system. The timing diagram of ADCS7476 [44] is shown in fig. 3.4 in which first 4 zeroes are not considered and

the remaining 12 binary values corresponds to the analog value. The process of sampling is originated at every rising edge of the clock and then applied at the line sample. When reset is given all the data in spdata2 shift register and counter count will be cleared. When clk is at raising edge counter will starts upward counting. If count is above '3' and raising edge of clk is applied then input sdata 2 (serial data) will be forced on to spdata2 shift register LSB. When count reaches "15" then data in shift register will be reflected parallel on to pdata2 that is a 12 bit bus. At that, time cs will be active high signal. Pclk will be at active high signal for above count of '8'.

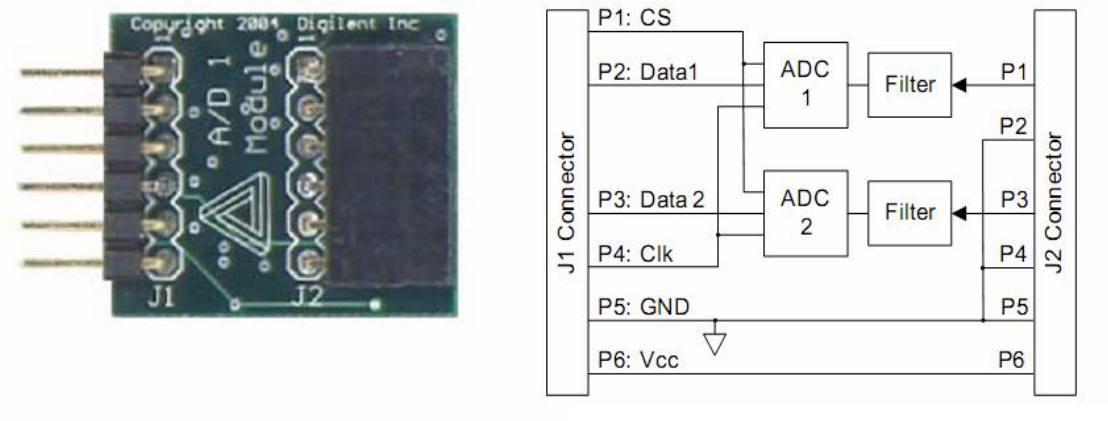

Fig. 3.5 (a) PMOD connector and (b) Interconnections [63]

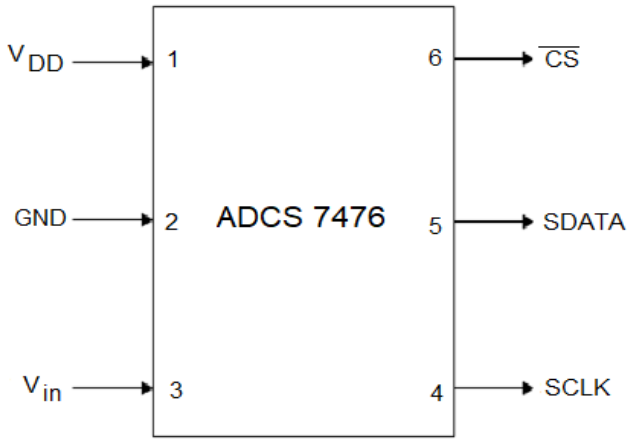

Fig. 3.6 Pin description of ADCS 7476

FPGAs holds good for the purpose of serial ADC. The reason behind serial interface communication is it consumes less line while the FPGA are fast to build the high-speed serial communication data. The fig. 3.5 shows the interconnections of inbuilt ADCS7476MSPS [44, 45] offers faster speed and low power consumption, 12-bit A/D converter. ADC is a high-speed serial interface, which can be interfaced easily with FPGA. The ADC interface adapter (AD1_PMOD) is connected to FPGA. The detail of the ADC module ADCS 7476 chip input and output pins is show in in fig. 3.6 listed in table 3.1.

Table 3.1 Pin detail of ADC module ADCS 7476

S. No	Pin Name	Description
1	V_{DD}	Is the power supply input (2.7 V to 5.25 V)
2	GND	Is is used to ground return of power supply
3	V_{IN}	Analog Input value 0 to 3.3 V
4	SCLK	It is the digital clk input works on frequency (10 KHz to 20 MHz)
5	SDATA	It is the digital output data and received based on clock input signal.
6	$\overline{CS}$	Is is the conversion process for chip select and denotes the active low input.

The PMOD adapter converts the digital ECG samples from ADC is sent the data parallel to the next block.

3.1.3 Power line 50 Hz Noise Removal

The 50 Hz noise removal filter is used for removing the noise generated from the power line. The Notch filter using infinite impulse response is used to attenuate the

50 Hz signal. The functionality of the ECG is controlled by slide switch. If the switch is '0' then the ECG simulation analysis is carried out else real time ECG signal analysis is carried out. The 6-bit sine wave noise is added to the original ECG signal in the simulation mode and in the real time analysis, the 50 Hz noise is included through the wires connected to the ECG machine. Second order Infinite Impulse Response type digital filter employed with direct form -II is implemented and the filter coefficients are generated.

IIR filters are recursive type of filters, by implementing the direct form II less numbers of memory locations are required. If the transfer function H (z) having the M number of zeros and N number of poles then the maximum of (M, N) will be the memory locations in the IIR direct form II realization of filter whereas direct form-I will require M+N+1 memory locations.

The transfer function equation of the IIR digital filter is presented as

$$H(Z) = \frac{\sum_{K=0}^{M} \beta_K Z^{-K}}{1 + \sum_{K=1}^{N} \alpha_k z^{-k}} \qquad (3.1)$$

Where, β_K is the filter coefficient for numerator and α_k is filter coefficients for denominator.

3.1.4 Noise Removal Filter for High Frequency

The FIR filter is used for the Band Pass Filter (BPF) as high frequency noise removal filter [31]. The BPF allows the lower frequency being 0.05 HZ and the higher frequency being 100 Hz, the band of frequencies. FIR filters are always stable filters and often implemented using the non-recursive structure that is no feedback is required. The output behavior and response of the FIR type filter is depending on the present inputs and the previous sampled inputs. The system function or the transfer function of the FIR filter is given as

$$H(Z) = \sum_{n=0}^{N-1} \beta_k \, z^{-n} \qquad (3.2)$$

Where, β_K are the filter coefficients in the numerator FIR filter coefficients can be computed by using the different windowing techniques for example rectangular window, which is used in faster rolling off in the frequency domain representation. It will have a minimum attenuation in the stop band beside that it will have a poor group delay characteristics. The another type of the window that is Blackman window have a good attenuation in the stop band and also group delay, but its limitation is the wide range of the transition band bandwidth between the frequency attenuation floor and the corner frequency apart from the above limitations the windowing techniques will not optimize the design. Optimization means to have the minimum filter coefficients, which can be efficiently removes, the noise that is associated with the ECG signal.

3.1.5 FIR Filter

Many of the Digital Signal Processing (DSP) systems are following the FIR filters as basic building block. The main reason to prefer FIR filter [67] for DSP applications is that the filters have linear phase and stable properties. The key use of the FIR filter is to remove and filter out unwanted regions of the input signal. It provides the shape to the signal after filtering in a communication channel. The main building blocks and components of FIR filter are adders, multipliers and delay elements. All the components can be arranged systematically in the FIR structure depending on the architecture and different forms of structure realization. The output of FIR filter is a linear convolution sum can be performed over a window of 'N' length or data samples with N-1 tap coefficients. Mathematically, for input sequence x(n) and length h(n) , the filter output y(n) is expressed as given in eqn(3.3)

$$\boldsymbol{y(n) = x(n) \otimes h(n)} \qquad (\mathbf{3.3})$$

$$\boldsymbol{y(n) = \sum_{k=0}^{N-1} h(k)x(n-k)} \qquad (\mathbf{3.4})$$

The direct form structure implementation can be done using FIR filter direct structure and easily developed using convolution sum. For N = 5, the can be written as

$$\boldsymbol{y(n) = \sum_{k=0}^{4} h(k)x(n-k)} \qquad (\mathbf{3.5})$$

$$y(n) = h(0)x(0) + h(1)x(n-1) + h(2)x(n-2) + h(3)x(n-3) + h(4)x(n-4) + \ldots\ldots\ldots\ldots\ldots\ldots h(n-1)x(n-1) \qquad (3.6)$$

The direct form of FIR filter can be changed is to it's alternate and opposite structure called transposed form of FIR filter. This transposed form will exchange the input samples and output samples and reversing the signal flow direction by adding an adder element in the same form and vice versa in comparison to direct form. The FIR filter with transposed structure is used to implement in the FPGA hardware. The advantage of this filter is that it does not requires any additional pipeline stages for the adder elements associated with the multipliers for getting the high throughput. The propagation delay in the transposed structure is also less in comparison to direct form from staring point to end.

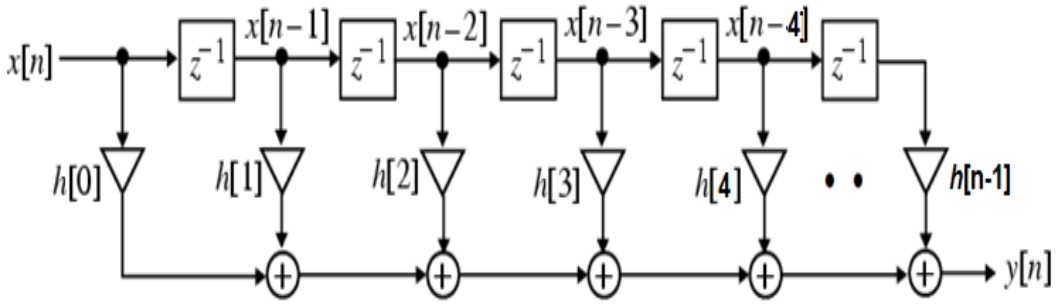

Fig. 3.7 Direct form structure for FIR filter.

The realization of FIR filter over length 'n' using direct form and transposed form is shown in fig. 3.7 and fig 3.8 respectively. Where, x(n) = {x(0), x(n-1), x(n-2)……x(n-1)} are the input values of the filter and h (n) = {h(0), h(1)……h(n-1)} are the filter coefficients, corresponding to input values. The term z^{-1} is related delay element and stored in the memory and y(n) presents the output samples after filtering operation.

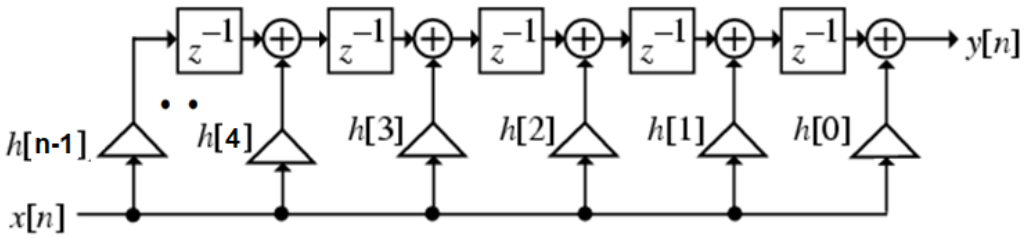

Fig. 3.8 Transposed form structure for FIR filter.

The output obtained from the Notch filter is given to high frequency noise removal filter. This filter is employed to attenuate signals which are not lying the in the frequency range of 0.05 Hz to 100 Hz, allows these frequencies only.

3.1.6 Dual Port RAM

The main operation of the RAM memory is to perform read and write operation in memory register and banks synchronize by clock signal. In single port memory, either writing or reading is possible at one time on single port based on address. The dual Port RAM has two ports and data writing and reading is happening on both port but following single clock. The functionality of single port RAM is shown in fig. 3.9 and timing in fig. 3.10.

Memory Read: The process of reading the source and destination operands or words with respect to register address is called memory read operation.

Memory Write: After reading the data or operands data is stored at particular memory location or address of register, is called the write operation.

In the processor operation, first memory read operation occurs and then write operation. The memory unit receives the address of the registers from the address lies, called the address register (AR). The contents of the registers are transferred to another register, referred as data register (DR). Then read operation is represented as

$$\textit{Memory Read: } DR \leftarrow M\,[AR]_{source} \qquad (3.7)$$

The contents of data register are transferred to memory unit at specified address, during write operation. Assuming the input data memory connects is in R2 register and corresponding address is in AR register.

$$\textit{Memory Write: } M\,[AR]_{destination} \leftarrow DR \qquad (3.8)$$

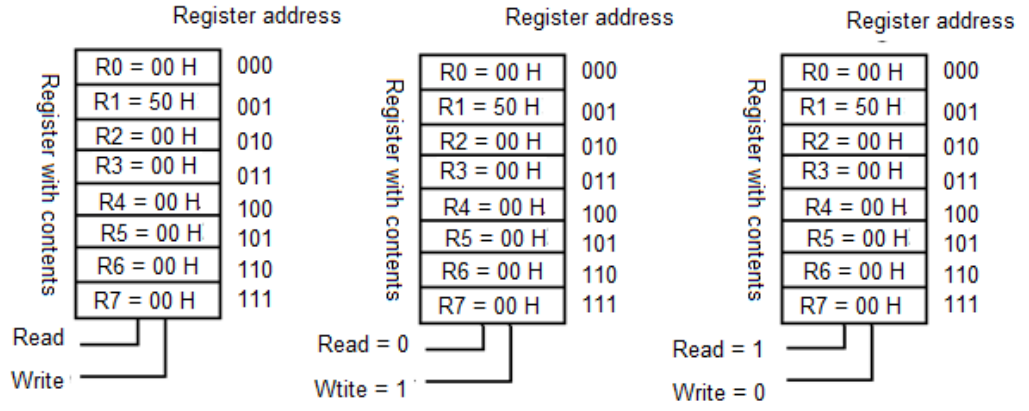

Fig. 3.9 (a) Initial stage (b) Memory read operation (c) Memory write operation

Memory read: R2 ← R1 or DR (address = 010) ←M [AR] $_{source}$ (address = 001)

Memory write: R2 ← R1 or M [AR] $_{destination}$ (address = 101) ←DR (address = 010)

It can be understood with the help of RAM memory array which has 8 registers (R0- R7) with addresses (000,001,010,011,100,101,110,111), having the data contents 00H, 50H, 00H, 00H, 00H, 00H, 00H,00H. During the first cycle of clock, let we want to fetch the instruction from R1 (001) register which is called source

memory address M[AR] $_{source}$ register having data 50H stored temporarily in R2 (010) register called memory data register (DR), for memory read Now R2 Register will have 50H. R2 data is stored in R5 (101) register or M [AR] $_{destination}$ during memory write operation. Now R5 Register will have 50H and R2 register will have 00H.

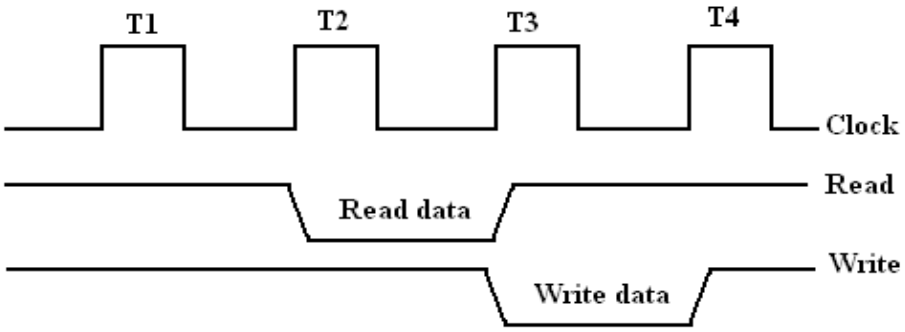

Fig. 3.10 Memory read and write operation

In the dual port RAM, data writing will happen at port-1 and data reading will happen on port-2. The dual port RAM diagram is shown in fig. 3.11 and fig. 3.13, in which wrire_enable is at port-1 and read_enable is at port-2. The port1 is following write_clk and port as read_clk but the duty cycle of both clk is same and synchronized with each other. First Input First Output (FIFO) logic is used to assign the priority of writing and reading the contents corresponding to port1 and port-2 and write_point and read_pointer is pointing the address of the memory locations to write and read the data corresponding to port-1 and port -2. Write_data and Read_data is the data should be written or read in the memory ports.

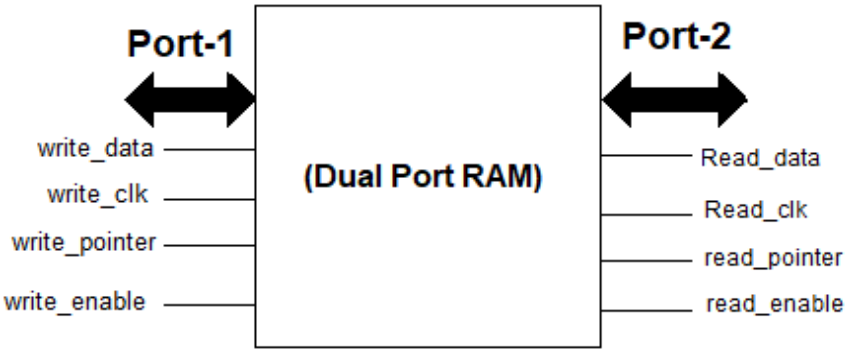

Fig. 3.11 Dual Port RAM

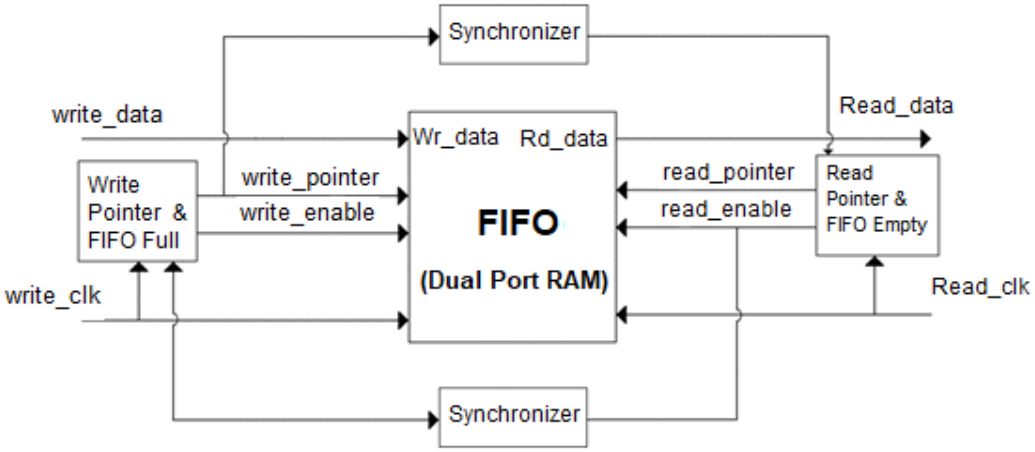

Fig. 3.12 Dual Port RAM data synchronization

The output from high frequency noise removal filter is given to block ram. The binary coefficients of filter are generated by copy coefficients of the PFIR package and storing them in the PFIR package by changed names as filter_notch for notch filter operation and filter_bpf for band pass filter as high frequency noise removal filter. The generation of ECG signal depends on the system simulation mode and switch present in the FPGA and patient data available on physionet.org [38]. The data is buffered in a dual port RAM. The write port is associated with the noise removed ECG signal. Read port reads is used to read this data and provides it to the FFT block. The patient 1 details are taken and MATLAB can be used for simulate and develop the converted data in the workspace to binary format according to specified length i.e 12 bit data length of ECG signal. The values, which are generated in the binary equivalent format, is copied and then saved in the ECG dual port RAM block. As the clock signal is forced then all the values are sent to the output, which will result the ECG signal.

3.1.7 Short Time Fourier Transform (STFT)

STFT is the Fourier related transform used to determine the sinusoidal frequency and phase contents of local parts of the signal changing with respect to time. The longer time signal is divided into smaller segments of equal length and then

applying the Fourier transform separately on each small segment. It presents the Fourier spectrum for each small segment and then plats the spectrum with respect to time. In discrete STFT, the data is distributed into frames or chunks. Each chunk is Fourier transformed and complex results are used to determine the magnitude and phase of individual point the signal with respect to time and frequency. The 2D STFT can be expressed mathematically by equ. (3.9)

$$\text{STFT, } x[n](\mathrm{m},\omega) = \mathrm{X}(\mathrm{m},\omega) = \sum_{n=-\infty}^{\infty} x[n]\omega[n-m]e^{-jwn} \qquad (3.9)$$

Where x(n) is the input, $\omega[n]$ is the window function. Here 'm' is discrete and 'ω' is continuous in nature. The STFT will divide a time domain signal into the smaller segments of equal length and then computing the FFT on each of the smaller segments. In case of FFT we have to consider Here m as discrete and ω as quantized. The Magnitude of STFT as a function of spectrum is given by equ.(3.10)

$$\{\mathrm{x(t)}\}(\tau,\omega) = |X(\tau,\omega)|^2 \qquad (3.10)$$

Where τ presents the phase delay.

3.1.8 Fast Fourier Transform (FFT)

The fast Fourier Transform (FFT) is an algorithm that efficiently computes the discrete Fourier Transform (DFT). The DFT of sequence x(n) over length N is given by the relation which is a complex valued sequence X(k). The basic equation for the FFT calculation, i.e. convert the input samples in to the frequency domain from time domain is given by

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} \quad Where\ 0 \leq\leq N-1 \qquad (3.11)$$

The equation is also presented as

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} = \sum_{n=0}^{N-1} x(n)W_N^{nk} \qquad Where\ 0 \leq k \leq N-1 \quad (3.12)$$

Here W_N represents the complex valued phase factor, which is the N^{th} root of unity and expressed as $W_N = e^{-j2\pi/N}$. The basic building blocks of FFT implementation are Adder, Multiplier, Butterfly structure and Twiddle factor multiplier. There are two types of Radix-2 FFT [7] algorithms: Decimation in Time (DIT)-FFT and Decimation in Frequency (DIF)-FFT. Both the transformations rely on the recursive decomposition of an N point transform into two (N/2) point transforms. This decomposition process can be applied to any composite (non-prime) N. The method is easier if N is divisible by 2 and if N is a regular power of 2, the decomposition can be applied repeatedly until the trivial '1 point' transform is reached. The radix-2 decimation-in-frequency FFT is an important algorithm obtained by the divide-and-conquer approach [90]. The Fig. 3.13 reveals the first stage of the 8-point DIF algorithm.

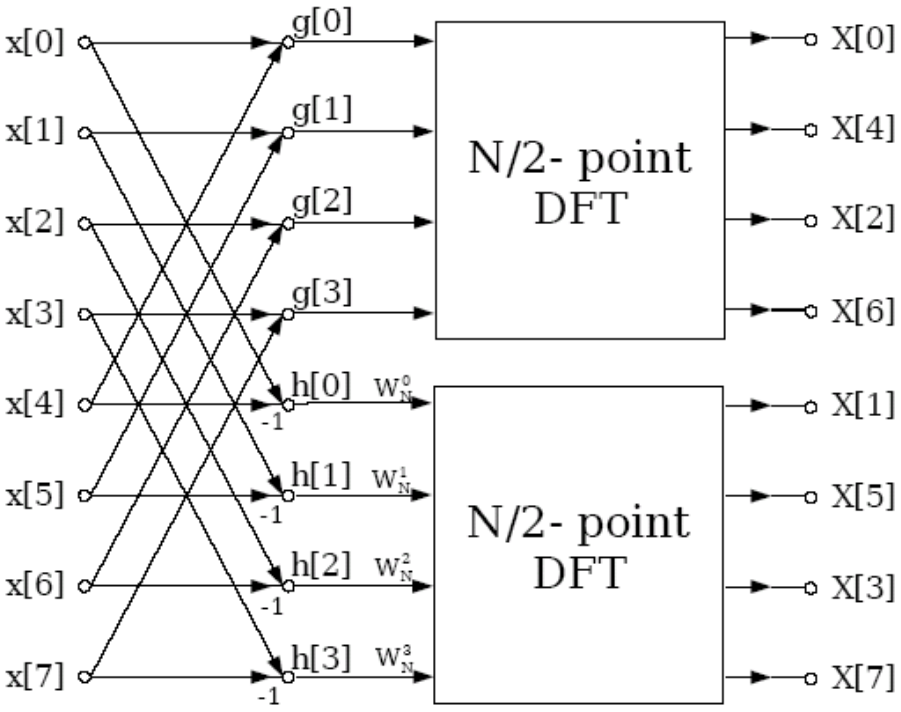

Fig.3.13. First stage of 8-point Decimation in Frequency FFT algorithm

The decimation, however, causes shuffling in data. The entire process involves v = $\log_2 N$ stages of decimation, where each stage involves N/2 butterflies of the type shown in the Fig. 3.14

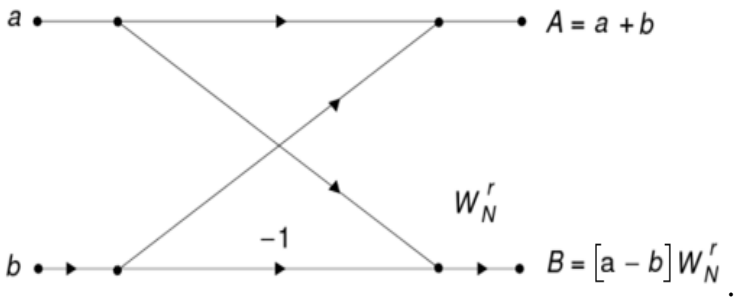

Fig.3.14 Butterfly structure of Decimation in Frequency FFT algorithm

Here a, b are the input points, A, B are the FFT output points in frequency domain, W_N is the twiddle factor .Consequently, the computation of N-point DFT via this algorithm requires (N/2) $\log_2 N$ complex multiplications.

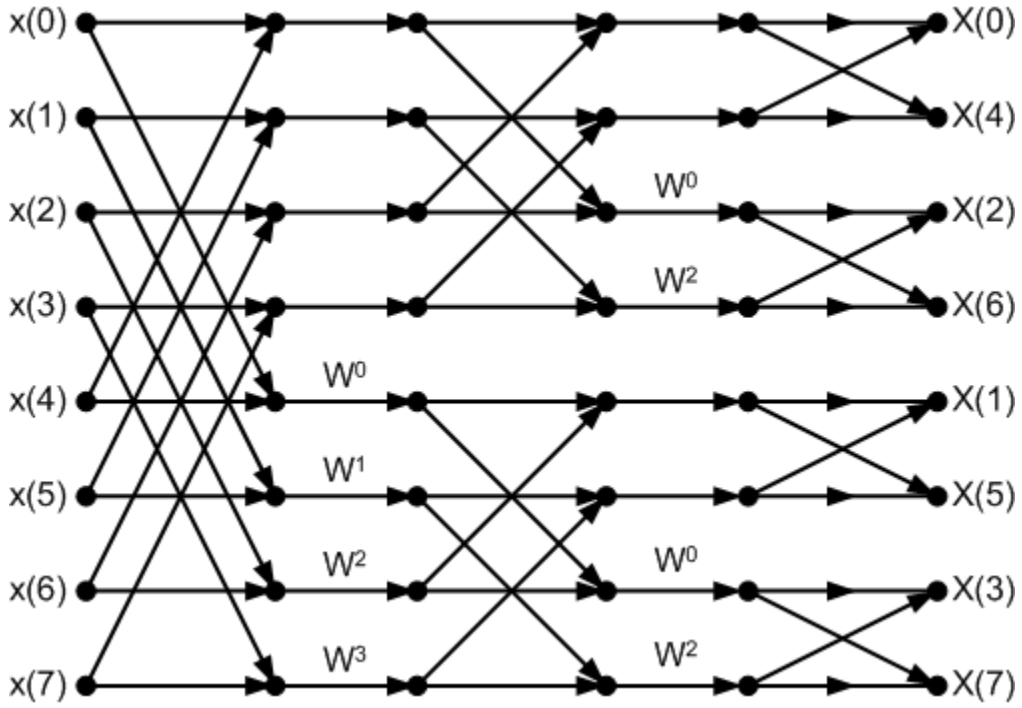

Fig.3.15 Structure of 8-point Decimation in Frequency FFT algorithm

For illustrative purposes, the eight-point decimation-in frequency algorithm is shown in the Fig.3.15. We observe that the output sequence occurs in bit-reversed order with respect to the input. Furthermore, if we abandon the requirement that the computations occur in place, it is also possible to have both the input and output in normal order. The 8-point sequence Discrete Fourier transform requires 64(N^2) complex multiplications and 56(N (N-1)) complex additions where as Fast Fourier transform requires (N/2) $\log_2 N$ number of complex multiplications

$\frac{8}{2}\log_2^8$ = 4*3 $\log_2^2$=12 complex multiplications and N $\log_2 N$ complex additions which implies $8\log_2^8$=8*3$\log_2^2$=24 number of complex additions. As shown in the above butterfly structure in figure 3.11, 8 point sequence of FFT requires 3 stages similarly 1024 point sequence requires the 10 stages and it requires 5120 complex multiplications and 10240 complex additions. The speed improvement factor as compared to DFT, FFT is 205 times faster for multiplications and it is 103 times faster for additions which is illustrated in the below

Speed improvement factor for multiplications is given by $\frac{N^2}{(N/2)\ log_2 N}$ (3.13)

Speed improvement factor for additions is given by $\frac{N\ (N-1)}{N\ log_2 N}$ (3.14)

After the noise, removal part the FFT block will compute the 1024-point FFT for the ECG signal the FFT will contain the real and imaginary values. There is chance of overlapping if directly FFT is performed the alternate solution is to use the STFT. The STFT the special type of FFT where the large sequence is sub divided into the smaller sub sequences in order to remove the overlapping of samples in the frequency domain representation. STFT with 256 point FFT is calculated for every 50 ms in the time domain representation to get the exact frequency components of the ECG signal.

3.1.9 2D- FFT Realization for 1024 point

2D-FFT algorithm is implemented by using two shorter length FFTs (lengths N1 and N2) to calculate an FFT of length N = NI xN2 [68]. The two-dimensional (2D) FFT of N= N_1X N_2 is defined as follows as shown in the equation (3.15).

$$X[k_1N_2+K_2]=\sum_{n_1=0}^{N_1-1}\left[e^{\frac{-j2\Pi n_1k_2}{N}}\left(\sum_{n_2=0}^{N_2-1}X(n_2N_1+n_1)e^{\frac{-j2\Pi n_2k_2}{N_2}}\right)\right]e^{\frac{-j2\Pi n_1k_1}{N_1}} \tag{3.15}$$

The design about variable point FFT processor is just based on FFT module . According to the idea of two-dimensional Fourier algorithm, i.e. if N = 128, then N1 = 2, N2 = 64, From 128 = 2 * 64 ,We find that when one wants to achieve 128-point FFT, Firstly the data is arranged in 64 lines and 2 rows, Secondly the input data will transform the 64 points FFT, then the result multiplies with the twiddle factor, Thirdly, let the result do 2 point FFT between 64-pt and 2-pt FFT outputs. Similarly, Calculation of the 512-point FFT firstly do the 64 points FFT, then transform further 8 points FFT . The same way to calculation of the 1024 FFT is implemented. Block diagram of the overall design of the FFT processor is shown in Fig.3.16

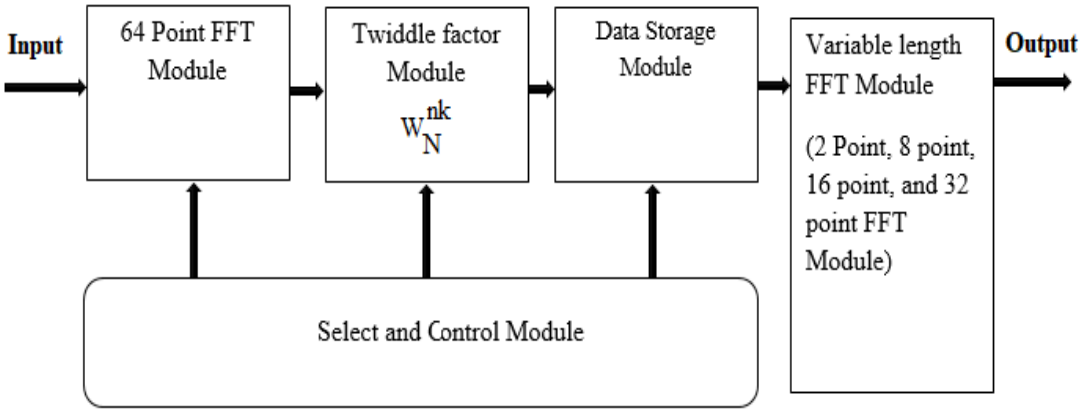

Fig.3.16.Block diagram of the overall design of the variable length FFT processor

The 64 point FFT is also implemented in 2-Dimensional FFT fashion using 8-point FFT modules as the kernel part using pipeline and parallel execution concept. This module is the most frequently used in the design. Four kinds of input data length all must first pass through the 64 points FFT module. Block diagram of this part is shown in Fig.3.17. The same idea to implement the 64-point FFT in the module based on 2D Fourier transform algorithm is composed of two 8-point FFT modules [71].

The 8-point FFT processor architecture consists of a single radix-2 butterfly (which is referred as the butterfly-processing element), a dual-port FIFO RAM, a coefficient ROM, a controller and an address generation unit.

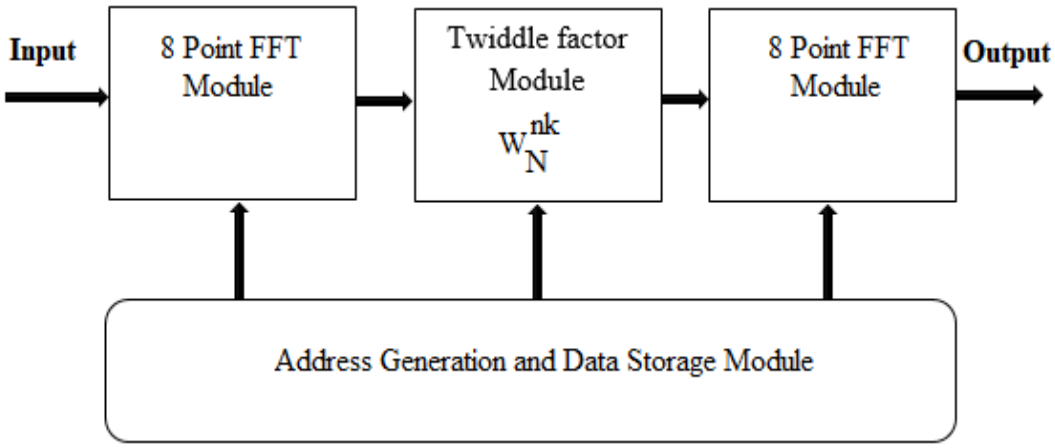

Fig.3.17 Pipeline structure of 64-point FFT Processor

The Fig. 3.18 shows the internal blocks of 64 point FFT module. The Input Buffer takes continuous data(x_in) and apply input clock as in_clk as shown in below diagram. This input Buffer performs as a SIPO (serial input and parallel output) i.e. it takes input as serial data and gives output as parallel. It will arrange the input data into rows and columns wise based on $(\mathbf{n_2N_1+n_1})$ Where $0 \leq n_2 \leq N_2 - 1$ and $0 \leq n_1 \leq N_1 - 1$. The Ping Pong Buffer contains two memory blocks. The memory blocks perform operation simultaneously i.e. one memory block writes the first FFT output and Second memory block reads the data from first FFT output and in the next

clock it will perform reverse operation i.e. first memory block reads, and another performs the write operation and again in next clock operations vice versa [72, 73].

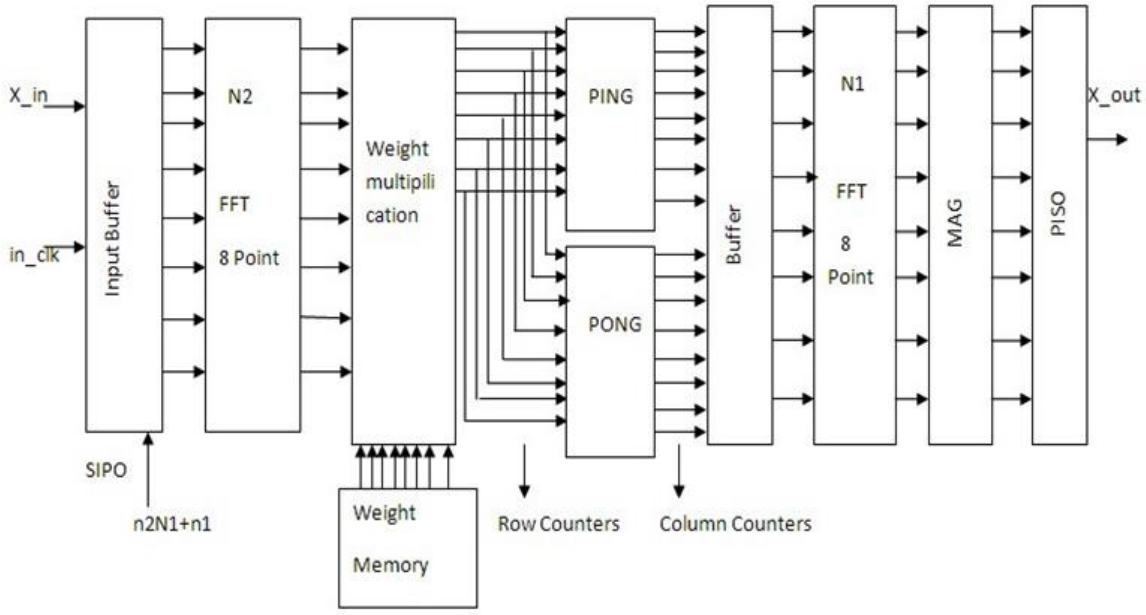

Fig.3.18 Internal Block diagram of the 64-point FFT module

Ping-Pong buffering increases memory bandwidth by a factor of two. Ping-pong buffering halves the number of memory operations per unit time, allowing faster buffers to be built from a given type of memory. Alternatively, for a buffer of given bandwidth, ping-pong buffering allows the use of slower, lower-cost memory devices. But ping-pong buffers have disadvantage that they waste a fraction of the memory. The overflow rate is increased until the additional memory is used half of the memory is wasted in the worst case. This can be compensated by doubling the size of the memory. Fig.3.19 shows a ping-pong buffer of total capacity M cells, with the arrival and the departure processes denoted as A and B, respectively. The buffer consists of two physically separate memory devices, each of size M/2. The two memories are arranged in such a way that from the outside, they appear to be a single buffer. Read and Write operations can take place simultaneously in a ping-pong buffer, but only in physically separate memory devices. When a cell arrives

and finds that one memory is being read, as shown in Fig.3.20, the arriving cell is directed into the other memory device. We call this type of write operation a 'constrained write'; we have no choice into which memory to write the arriving cell.

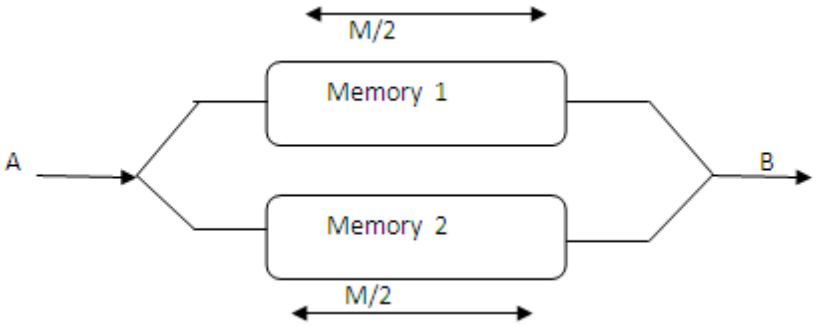

Fig.3.19 PING PONG memory

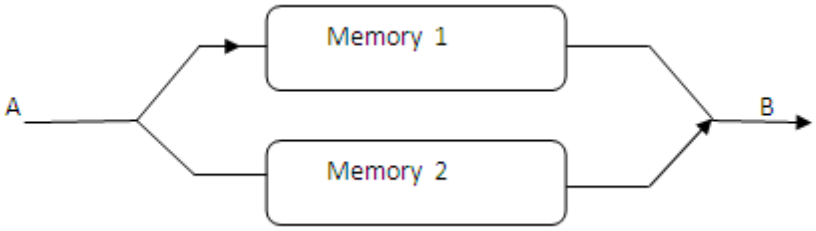

Fig.3.20 PING PONG memory Read and Write operations

If Ping Pong memory writes the output data in to the buffer as column wise means it will send the data as parallel to the next buffer. This buffer arranges complete data as rows and columns wise. It will send the first column to the N_1 point FFT i.e. 8 point FFT which is the kernel module. This process continuous up to last column .The output of N_1 point FFT can be perform magnitude operation i.e. Real ^{2}+imaginary^2= magnitude in the Magnitude block and send output to output Buffer which is PISO (parallel input and serial output). Since it works on high frequency, it will send the output as serially. This can be achieved by applying clock whose clock rate is 64 times faster than input clock. Finally the data is captured at the output serially.

As mentioned above, the result multiplies with twiddle factor, and performs 2 point-FFT with the result, Finally 128 point FFT is achieved. Similarly, Calculation of the 512-point FFT firstly do the 64 points FFT, then transform further 8 points FFT; The same way is used to calculate the 1024 and 2048 points FFT. Select and control module is also the kernel part to complete the alterable data length in the current dissertation. It is based on the input data points to select the results stored in data memory and choose the next flow. A two bits signal 'mode' is chosen as the mode signal simply as 4X1 Multiplexer to which mode 00, mode 01, mode 10, mode 11 will be the inputs. When mode = 00, means to choose 2 points FFT module, to complete the 128-point FFT; when mode = 01, means to choose 8 FFT module, to complete the 512-point FFT; Equally: When the mode = 10, means to completed 1024 point FFT; when mode = 11, means to complete the 2048 point FFT.

3.1.10 Magnitude Calculation

The output of the FFT is the real signal and imaginary signal; the magnitude block performs the absolute value of the input signal. The magnitude of the signal can be computed with the equation $\sqrt{(\text{Real})^2 + (\text{Imag})^2}$ Where Real stands for the real value and image is the imaginary value of the FFT signal.

$$Magnitude, \qquad M = \sqrt{(Real)^2 + (Imaginary)^2} \tag{3.16}$$

$$Phase, \qquad \varphi = \tan^{-1}\left(\frac{Imaginary}{Real}\right) \tag{3.17}$$

3.1.11 Chipscope Analyzer

Chipscope pro analyzer is used for the on chip verification in the FPGA. The bit stream file that is generated is dumped to the FPGA. From the FPGA all the signals are analyzed like ECG signal without noise and ECG signal with noise, the output of the FFT is also observed through the FPGA.

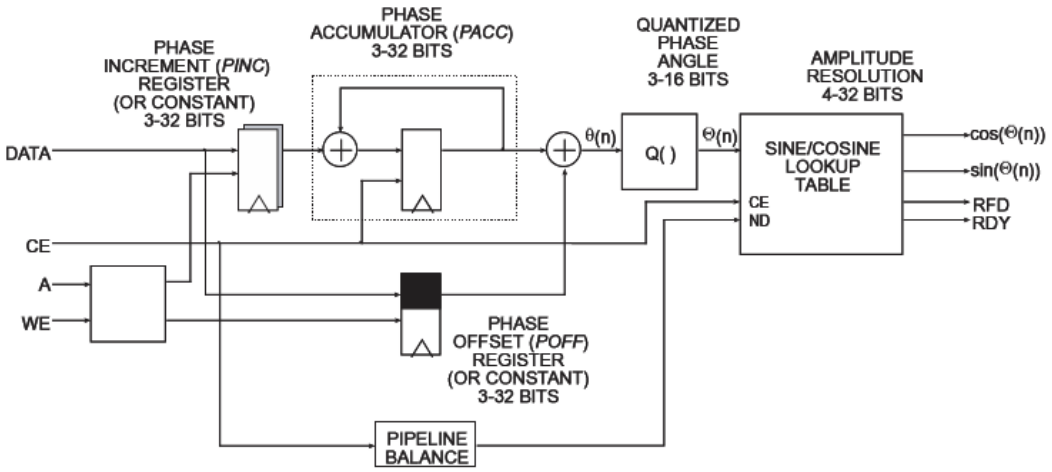

Fig.3.21 Chipscope Analyzer with DDS core

Digital Synthesis (DDS) provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation instead of using function generators. DDS is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

DDS devices like the AD9833 are programmed through a high-speed serial peripheral- interface (SPI), and need only an external clock to generate simple sine waves. DDS devices are now available that can generate frequencies from less than 1 Hz up to 400 MHz (based on a 1-GHz clock). Because a DDS is digitally programmable, the phase and frequency of a waveform can be easily adjusted without the need to change the external components that would normally need to be changed when using traditional analog-programmed waveform generators. DDS permits simple adjustments of frequency in real time to locate resonant frequencies or compensate for temperature drift. The core consists of two main parts, a Phase

Generator and SIN/COS LUT, which can be used independently or together with an optional dither generator to create a DDS capability. A time-division multi-channel capability is supported, with independently configurable phase increment and offset parameters. Fig.3.21 provides the block diagram of the DDS Compiler core.

CHAPTER-4
METHODOLOGY AND METHODS

The chapter explains the design methodology, different methods, R peak detection, QRS complex detection, filter design techniques. The chapter also discussed the different software tools description form simulation as well as synthesis. It also details the complete environment of functional simulation and logic verification.

4.1 Methodology for ECG Chip Synthesis

The block diagram of ECG Chip design, simulation and synthesis is shown in fig. 4.1. The steps of the process are discussed.

- ***Design Specification****:* There are two approaches in ECG system chip design one is bottom up design another is top-down approach. In the bottom up technique the design is developed for small modules and structured in a top design using structural style of modeling. In top-bottom up approach the full system is considered and designed in a way that it will meet the behavior of the system. In the ECG chip design, it is essential to define the cluster size and duty cycle of the clock input signal. The designer based on company project requirement decides the design specifications. In this design specifications are considered such as 12 bit ADC, 50 Hz noise removal filter 0.05 to 100 Hz, dual port RAM 32 KB and 1024 points FFT etc.
- ***HDL Modelling:*** The chip design is done using any of the HDL language. The industry favorite languages are Verilog HDL and VHDL. VHDL based design is used for the problem statement of our research because the ECG design can be modeled in dataflow modeling, behavior modeling or structured modeling

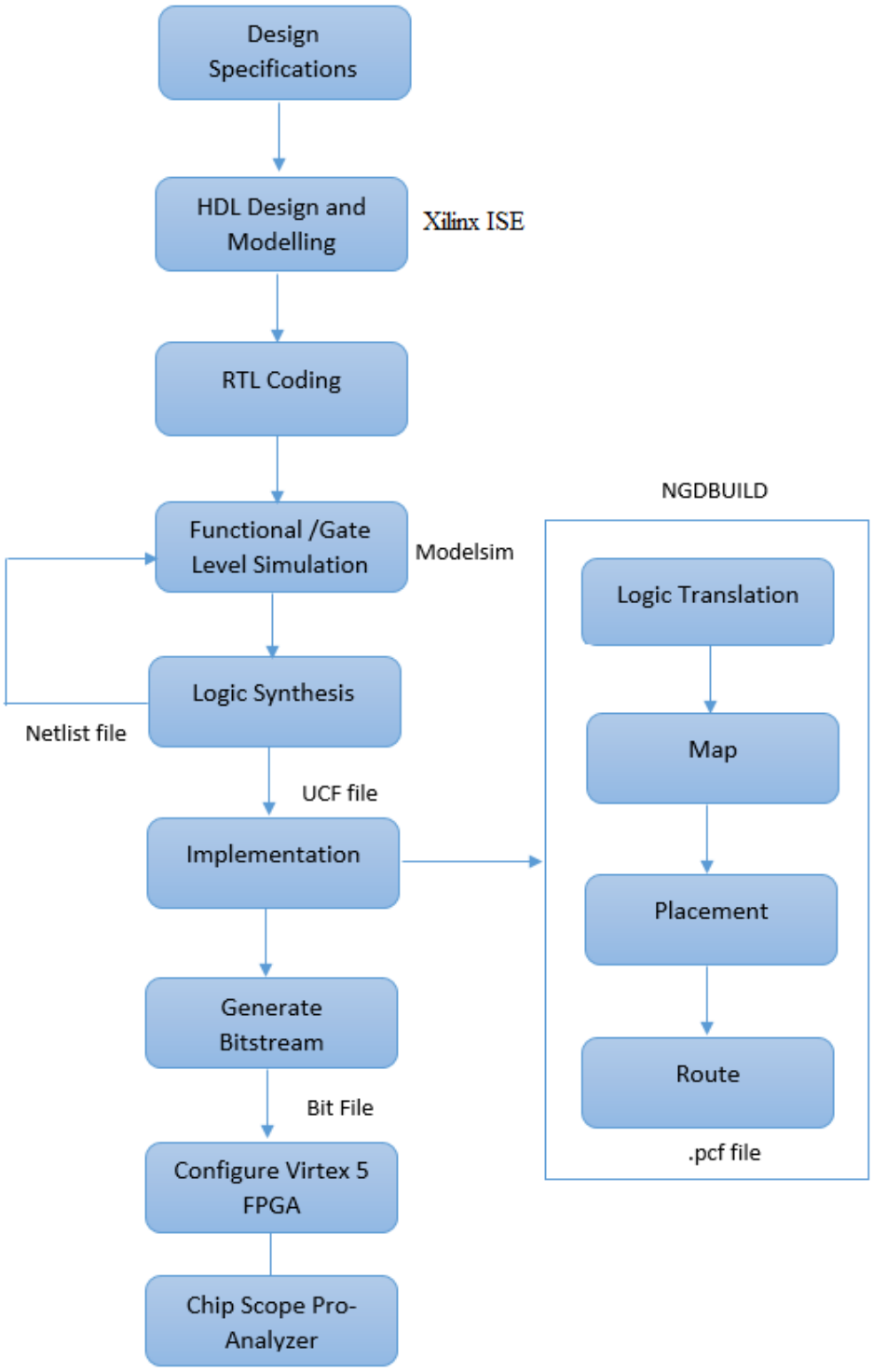

Fig.4.1 ECG System Design and Synthesis Methodology

using VHDL. In the VHDL Code, the designer can choose any one the style of modeling for the chip design.

Data flow Model – based on the logical expression output

Behavioral Model – based on system functionality and truth table

Structural Model – based on the architecture level design modules instances and interface

- ***RTL View:*** RTL is directly extracted from Xilinx Software and it is the graphical representation of the design (.ngr) is the file generated with the help of Xilinx Synthesis Technology (XST) where all the inputs and outputs of the top level module is observed. RTL view is the early stage of a synthesis process before the place and route process. The internal architecture of the processes and its behavior is checked. The design is represented in terms of multiplexers, adders, flip-flops, registers and so on.
- ***Functional Simulation:*** The functional simulation depends on reset circuitry, clock input and test cases. The designed chips and modules are checked by RTL view, internal schematic diagram and test cases. The designer based on the functionality of the designed chip decides test cases. RTL simulation or behavioral simulation is the timing simulation of the design, depends on the design hierarchy. The simulation is required for all the intermediate modules to under the behavior of chip for different test inputs before the synthesis to check the output waveform. In case of unsatisfied results, the designer has to go for redesign. VHDL or Verilog HDL is used in the behavioral simulation during the simulation level variables, signals are observed functions and procedures are traced and the breakpoints are set to check a sub module from the top-level module.
- ***Logic Synthesis:*** In the pre-synthesis, the ECG deigned chip performance is analyzed based on the hardware and timing parameters. The hardware parameters are slices, flip-flops, LUTs and memory requirements in the chip. The timing parameters are relating to combination delay, minimum time and

maximum time of clock etc. if nay chip design is consuming memory than 100 % utilization, then chip redesigning is required.

- ***Implementation:*** Based on the view synthesis report as the hardware and device utilization summary the designed modules are synthesized on FPGA. The FPGA is interfaced with the computer in which the code was developed for specific module. The test inputs are given using switches of the board and verified using LED, LCD or monitor using VGA. FPGA has the feature of inbuilt ADC and DAC conversion. So, FPGA synthesis and experimentation is required to test the designed chip in real time application. In the module, design experimentation is done on Virtex -5, high speed FPGA. The FPGA implementation process includes the logic translation and optimization on FPGA. The pre-synthesized code is required to burn in the core of FPGA that includes the process of technology mapping, placement and routing.

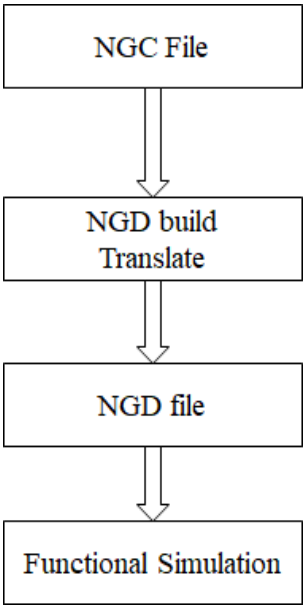

Fig. 4.2 FPGA translate

The User Constraints File (UCF) is created to configure the pins in Virtex 5, FPGA, then implementation is carried out. The implementation includes the technology mapping, placement and routing. The mapping reduces the blocks

to minimize the area and logic block are placed to provide optimal wire connection between cells called routing. NGDBuild ignores any invalid location constraints (LOC) information that would result in errors. Fig. 4.2 and Fig. 4.3 shows the logic translation and mapping in NGDBuild environment.

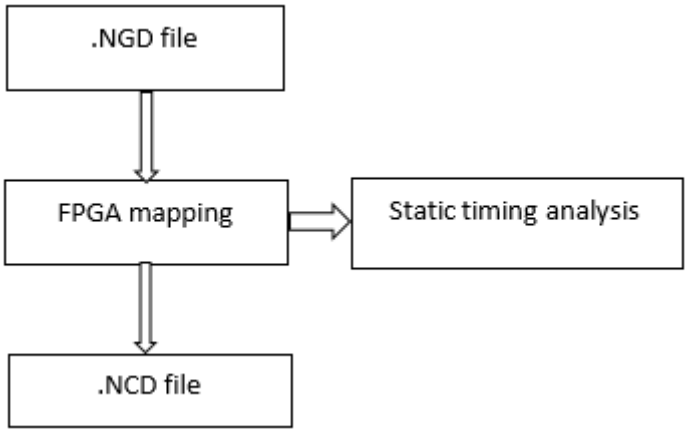

Fig. 4.3 FPGA Map

- ***Static Timing Analysis (STA):*** STA is the step after the mapping or placement and route processes. Post mapping the timing analysis of the report list the signal path delays of the design that derives from the logical design. After the PAR the timing information that incorporates the timing delays information which provides the detailed timing summary of the design. The analysis sis very much helpful to estimate the timing parameters oi FPGA such as minimum period, minimum time before clk signal, maximum timer after clk signal and total path delay.

- ***Bit File Generation:*** The design of the routed NCD file should be loaded into the hardware(FPGA) for this purpose the design should be converted into the format that is acceptable by FPGA. The FPGA burns the bit file in its core. The routed NCD file converts the bit stream file (.BIT file) to configure the targeted device in FPGA . The communication between the computer and FPGA can be

done using the JTAG cable or USB cable. These steps are followed after programming in the XILINX ISE.

- ***Configure Virtex-5 FPGA:*** In the process the code is configured to selected device in VirtexX5pro . In the design, XC5VLX110T is considered for the same purpose. The selected device should be matched with the device chosen during simulation and pre synthesis process in Xilinx ISE.
- ***Chip Scope Pro-Analyzer:*** Chipscope is the software based logical analyzer that is used for the on chip verification inside the FPGA device by properly incorporating the Integrated Controller (ICON) IP core, Integrated Logic Analyzer (ILA) core, Virtual Input Output (VIO) , Agilent Trace Core 2 (ATC2) and Integrated Bus Analyzer (IBA). All the internal signals from the design can be monitored or else any particular signal can be monitored.

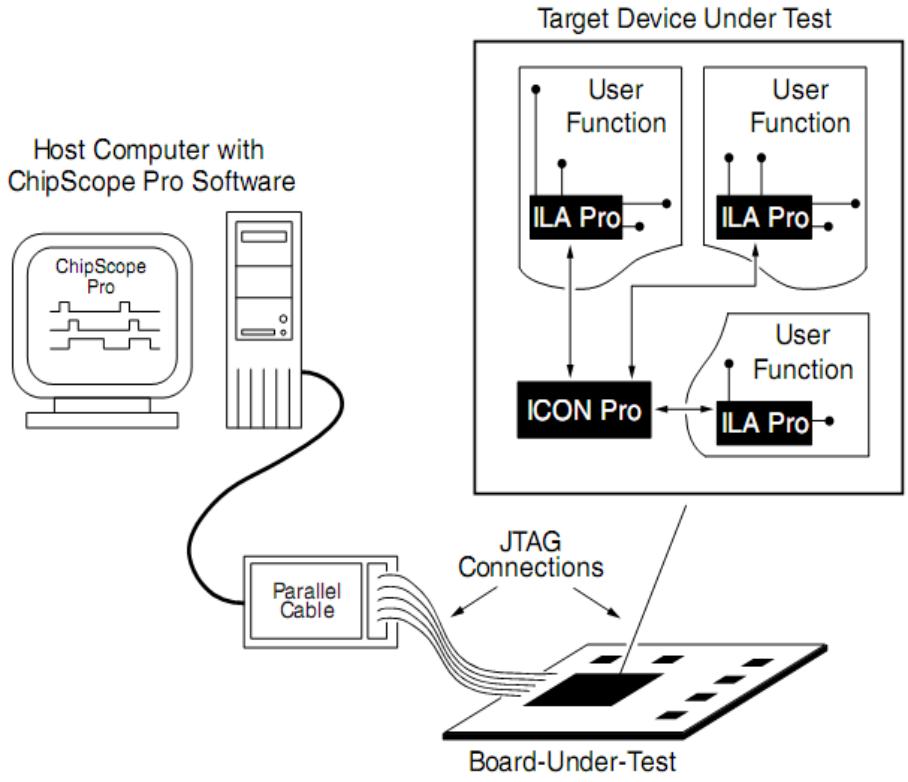

Fig. 4.4 Chip Scope Pro Cores Description

Chipscope provides the triggering options to view the output waveform. Fig. 4.4 shows the block diagram of the Chipscope pro analyzer [75] system for FPGA signal testing. The users can place the ICON, VIO, ILA, ATC2 and IBA IP cores collectively all will be calling as Chipscope pro cores. The design can be generated using these cores and instantiating into the HDL source code. With the help of tool core inserter all the IP cores for Chipscope can be directly synthesis of the design netlist. The IP-cores uses Joint Test Action Group (JTAG) boundary scan port for the communication between the host computer and the FPGA using the JTAG cable excluding the devices of virtex-5. For virtex-5 device. The ICON core follow either USER1 or USER2 for JTAG Boundary Scan programming instructions BSCAN_VIRTEX primitive and communicating with the device. ILA monitoring the triggering of inputs and outputs of the logic and recors the information of RAM resouces. It also control the status of output waveform.

4.2 Software Tools

The software used in the design of ECG chip implementation used is Xilinx ISE 14.2 and Modelsim 10.0 software

4.2.1 Xilinx ISE 14.2

Xilinx is one of the leading companies in the field FPGA design. It is the biggest semiconductor company to cover the front end solutions in the chip design, verification and synthesis. In the Xilinx software the programmers are developing the chip using latest HDL languages such as Verilog HDL, VHDL, ABEL etc. After the design there are the options to see the RTL, inter schematic view and view synthesis report. The developed chip is configured using input pins, output pins and input/output pins. Xilinx has the ISIM simulator to see the waveform using inbuilt waveform simulator which provides the functional check of the developed chip. It also has the Chipscope for FPGA signal analysis, Static timing analysis feature, verification and logical synthesis environment. Different test benches and test cases are simulated in the software environment and FPGA guarantees the chip for mask

production in the market. The tool provides the full information of logic design, synthesis, simulation, verification and timing analysis. The hardware and pre-synthesis parameters obtained directly from the tool which details the hardware parameters usage, memory requirements and timing values required in the design of chip.

4.2.2 Modelsim Software 10.1 Version

Modelsim Software is the software given by the Mentor Graphics Company. It is a multi-language HDL simulation software works on Verilog HDL, VHDL and System 'C'. It has the inbuilt 'C' debugger. It is preferred one of the best fool for GUI and Xilinx software interface. The chip design, functional simulation and timing analysis are done using the software. It also can be integrated with MATLAB or Simulink environment. The software gives the following advantages .

Benefits of Modelsim EE

- Modelsim software gives low cost chip design solution using HDL
- Providing interactive debug using Intuitive GUI in effective time
- It simplifies the research data and manages the project management integrated in software and hardware
- It has outstanding technical support to give the solutions in HDL and easy to use
- Easy to use with outstanding technical support
- Popular ASIC libraries are available and sign-off support for all defined libraries
- The complete platform for hardware and software debugging
- Simplifies the functional simulation and gives testing environment for all the possible test cases, can be used to check the functionality of the designed chip.

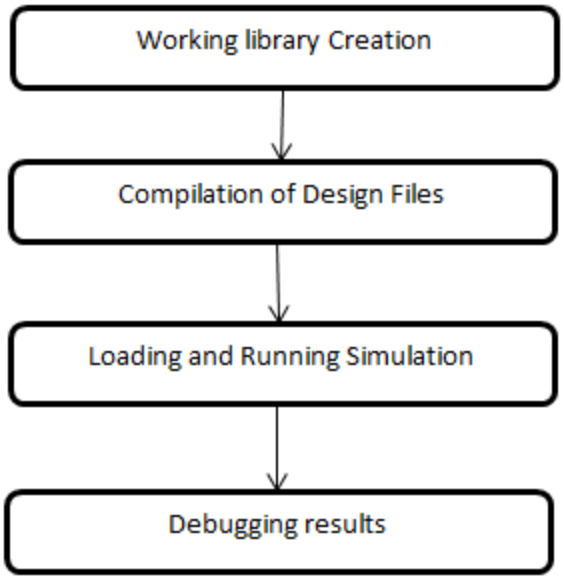

Fig. 4.5 Modelsim design process

The chip design flow and simulation block diagram using Modelsim software is shown in fig. 4.5

- ***Creation of working library:*** All the chip design based solutions in Modelsim software require the creation of the library. There is the default library in the Modelsim by the name 'work' which includes all the logical values and possible library functions required to do simulation by the compiler in the working library. The default destination of all the chip design is the library in Modelsim software.
- ***Designed file compilation:*** The designed which is developed using any HDL, and stored in the working library is complied. The binary created by the user is suited to work on all the platforms. The designed file may be one file or grouped as the top design having submodules or structured in bottom to top level.
- ***Running and loading Simulation:*** The designer is loading the top module of the developed chip into the simulator after completing the compilation of the design. The loading involves the entity of chip and architecture. The design can be done in dataflow, behavior and structural modeling. The modeling of the design is chosen by the designer. Some design structured using structure style

of modeling, gives better results. The design is developed in different modeling can give different timing and performance results. In the running process, it is considered that the simulation period is zero and run operations are entered by the designer to perform the functional simulation

- ***Results debugging:*** The developed chip may contain some errors. So, debugging environment is required to track the errors in program window. The errors are listed by the Modelsim software with respect to line and code debugging environment, help the program to check the code and take correction action in design. There are redefined scripts can be used in the software to follow the short methods. The verified results are seen in the form of waveform and timing diagrams.

4.2.3 MATLAB Signal Processing Tool

MATLAB signal processing tool box is used to preprocess analyze and extract the features of sampled signal. The toolbox has the resampling, retrending, smoothing, filter design and analysis (FDA), and power spectrum estimation features. The toolbox works on different functions used to extract features envelop detector-getting peaks on different patterns of signals. It performs measurements such as SNR, distortion and qualify signal similarities. It supports the signal analyzer to analyze and preprocess multiple signals parallel in time, frequency domain without writing any code. It explores large signals and extract regions of interest. It has the following features

- ***Signal Generation and Preprocessing:*** Signal creation, resampling, smoothing, noise removal, and detrending signals.
- ***Measurements and Feature Extraction:*** Signal statistics, peaks, power, pulse and transition metrics, bandwidth, distortion**.**

  Correlation and Convolution: Autocorrelation, Cross-correlation, auto covariance, cross-covariance, circular and linear convolution**.**
- ***Digital and Analog Filters Design:*** FIR and IIR filters, analysis, and implementation of filters, single-rate and multirate filter design.

- ***Transforms:*** Fourier Transform, Hilbert Transform, DCT, chirp-Z Transform, cepstrum, Walsh-Hadamard Transform**.**
- ***Spectral Analysis:*** Windows, coherence, and Power spectrum.
- ***Time-Frequency Analysis:*** Fourier synchro squeezing, spectrogram, time-frequency reassignment, cross-spectrogram, kurtogram
- ***Signal Modeling:*** Autoregressive (AR) models, linear prediction, Levinson-Durbin and Yule-Walker.
- ***Filter Design and Analysis (FDA) Tool .*** It is inbuilt toolbox with MATLAB signal processing tool to check the response with different windows techniques for filter design and getting quick response in tool itself. The common filters are low pass, high pass, band pass and band reject filters withy differentiators and integrators. The design method can be FIR or IIR based on design requirements. The response can be checked for 'n' order filter deign.

CHAPTER 5

FILTER DESIGN AND ECG SINGAL PROCESSING

The chapter explain the filter design in MATLAB Filter Design Analysis (FDA) tools for notch filer, band pass filter as FIR equiripple filter design. The MATLAB simulation results for ECG signal for different patients is also presented to analysis the R peak detection, and beats per minute.

5.1 MATLAB Filter Design Analysis (FDA)

The Filter Design Analysis (FDA) in MATLAB provides the simulation environment in which we can estimate the coefficient, system function simulation, FIR and IIR filter analysis and structure realization. The Fig. 5.1 shows the steps for filter coefficients generation. The generated filter coefficients will be in the fractional decimal notation. These values are converted into the 12-bit binary values.

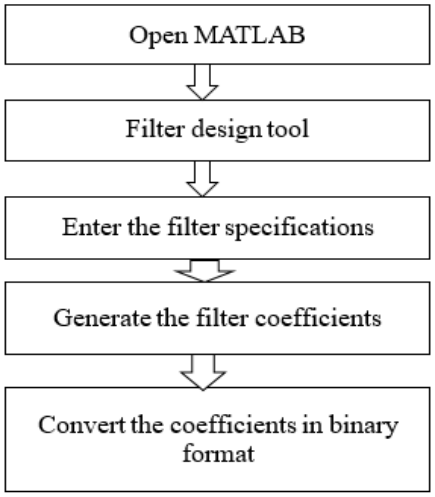

Fig. 5.1 Generating filter coefficients

5.1.1 Notch Filter Coefficients

The filter coefficients are generated for 50 Hz power supply frequency noise removal in MATLAB FDA tool. The filter coefficients are generated by MATLAB by given process below

Start → MATLAB → toolboxes → filter design HDL coder → filter design and analysis tool (FDA tool). Open FDA tool then select as shown in the fig. 5.2

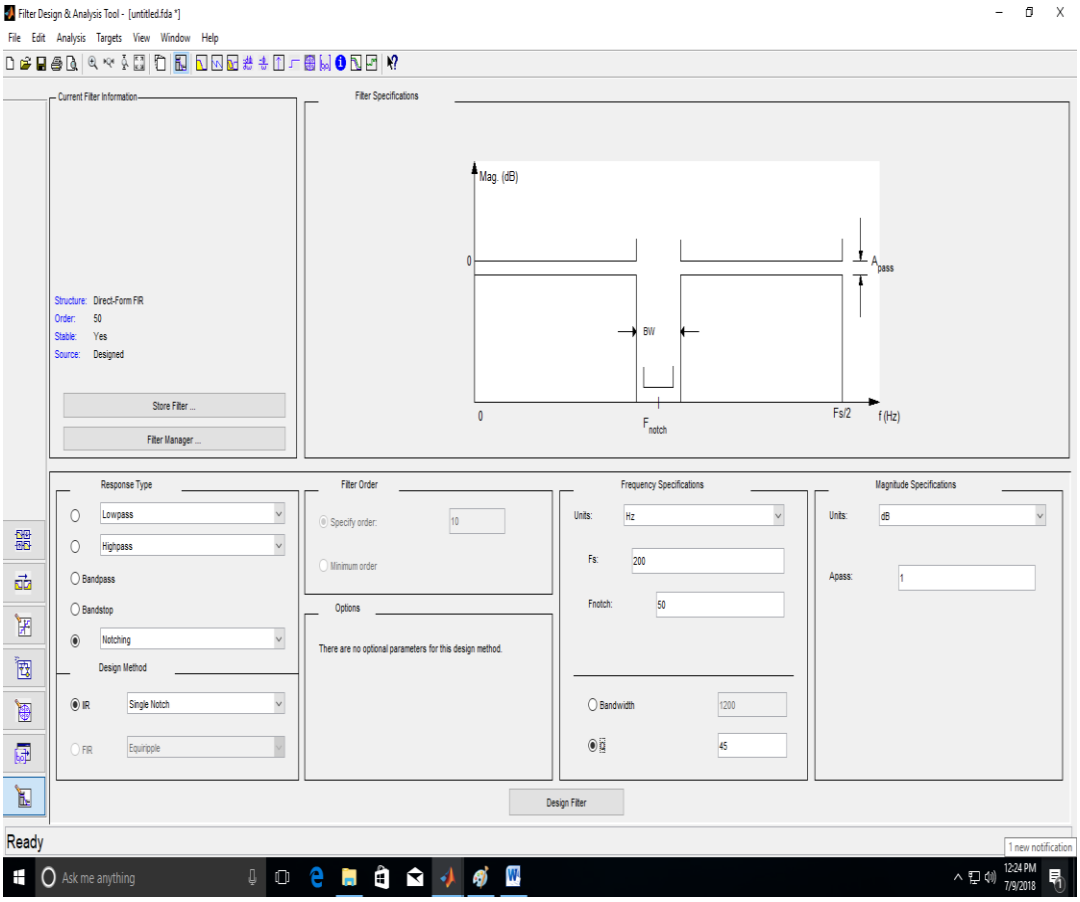

Fig 5.2 Filter coefficients

The FDA tool has the option to click on design filter. Then the coefficients will be generated as shown in the below fig. 5.3

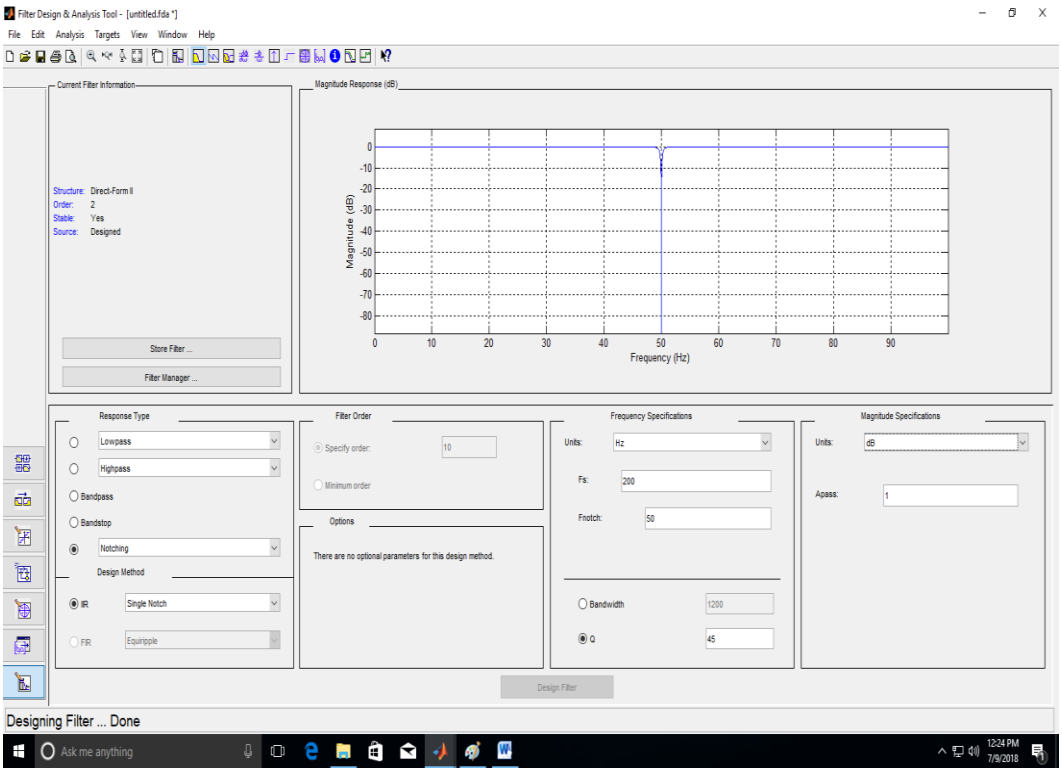

Fig. 5.3 Notch filter FDA tool

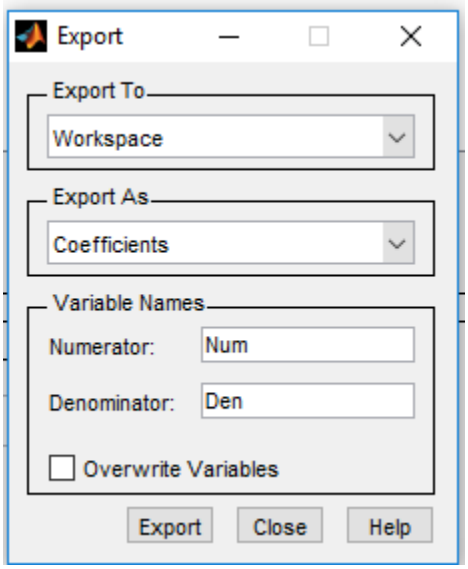

Fig. 5.4 Filter coefficients

The 50Hz noise removal filter is implemented to remove the power line interference [78, 79]. Notch filter using Infinite impulse response single notch and the quality

factor is 45 and the sampling frequency is 200 Hz is used to attenuate the 50 Hz signal. Fig. 5.4 shows the filter coefficients generated for the Open file select export, following window will be opened click on export, data will be exported to workspace. A MATLAB code, which converts the decimal numbers to binary values, taking the inputs from Mat Lab workspace (i.e. coefficients) and in the program total length of binary values and number of fractional parts in it. The transfer function of the IIR digital filters is of the form

$$H(Z) = \frac{\sum_{K=0}^{M} \beta_K Z^{-K}}{1 + \sum_{K=1}^{N} \alpha_k z^{-k}} \qquad (5.1)$$

Where, β_K is the filter coefficient for numerator and α_k is filter coefficients for denominator . The overall system function for the notch filter is given by equ.(5.2)

$$H(z) = \frac{0.99 - 0.001Z^{-1} + 0.991Z^{-2}}{1 - 0.001Z^{-1} + 0.98Z^{-2}} \qquad (5.2)$$

Where the sampling frequency is F_s = 200 Hz and the quality factor Q is given as 45.

5.1.2 High Pass Noise Removal filter.

The high pass noise removal filter is applicable in band 0.05 Hz to 100Hz. The filter specifications and simulation is shown in fig. 5.6. For high frequency noise removal filter , same steps are followed used for generating the coefficients of notch filer.

The band pass filter with the following specifications are used to remove the high frequency noise. The sampling frequency is set to 220Hz stop band filter of Fstop1 is chosen as 0.01Hz the pass band filter frequency of Fpass1 is 0.05Hz and Fpass2 is 100 Hz. The stop band filter Fstop2 is greater than 100Hz, Fstop2 is set as 101 Hz. Density factor is a parameter to control the density of the frequency grid set it as 16.

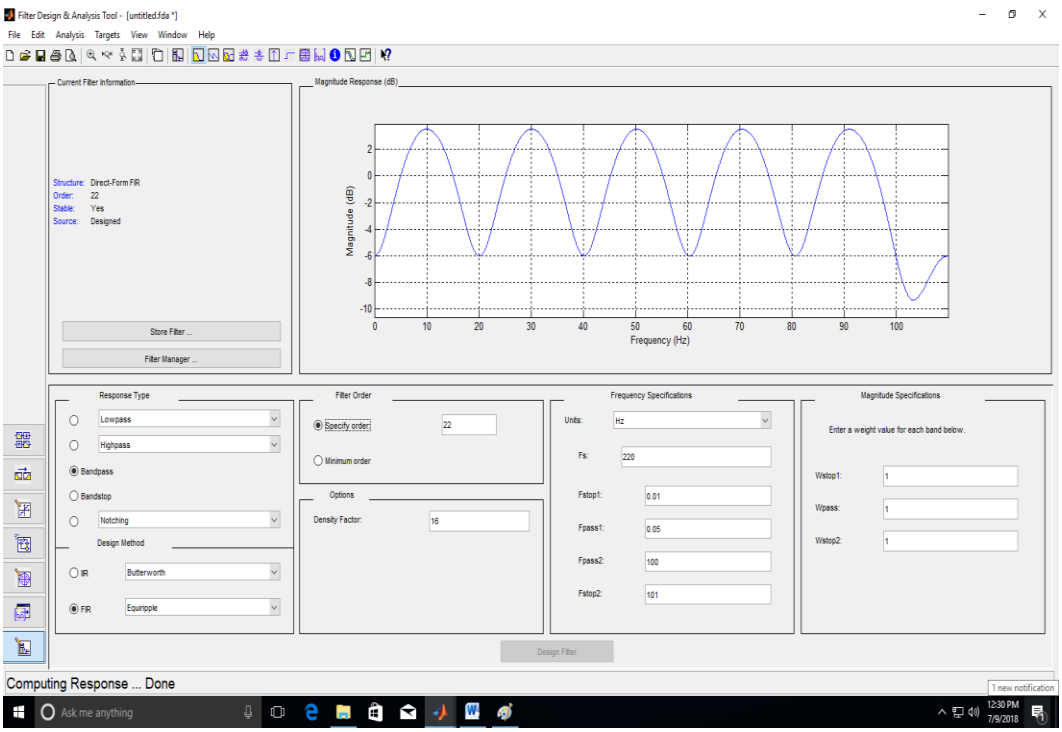

Fig 5.5 High frequency noise removal filter

5.1.3 FIR Filter Coefficients

The FIR filter is used for the Band Pass Filter (BPF). The BPF allows the lower frequency being 0.05 HZ and the higher frequency being 100 Hz, the band of frequencies The FIR filer coefficients are generated by band pass filter using the equiripple filter. This provides the alternate solution to the windowing technique with less number of filter coefficients. The method is based on the repetition process of comparing a selected coefficients set with the actual frequency response specified until the solution is obtained with fewer coefficients. Equiripple will have equal number of pass band and band stop as shown in fig. 5.6.

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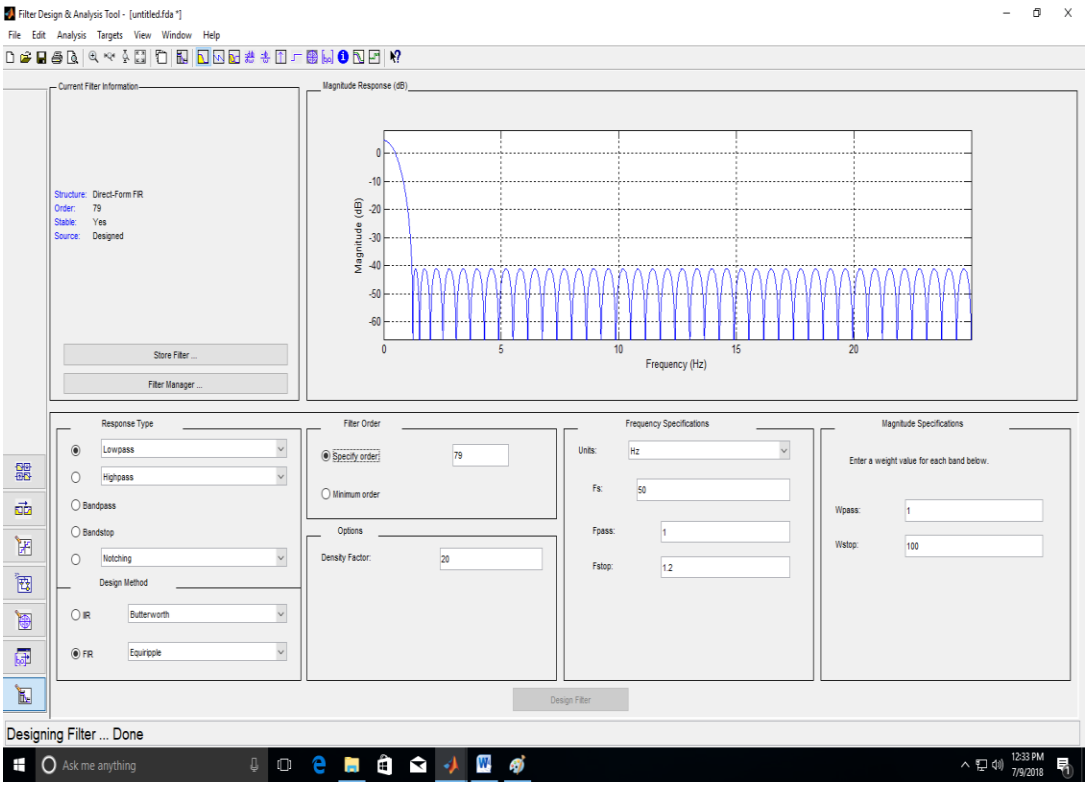


Fig. 5.6 Equiripple filter design

The BPF with the following specifications are used to filter the high frequency noises. The sampling frequency is set to 220Hz stop band filter of Fstop1 is chosen as 0.01 Hz the pass band filter frequency of Fpass1 is 0.05 Hz and Fpass2 is 100 Hz. The stop band filter Fstop2 is greater than 100 Hz, Fstop2 is set as 101 Hz. Density factor is a parameter to control the density of the frequency grid set it as 16. As the binary coefficients are generated copy coefficients to the PFIR package and save them in the PFIR package by different naming as filter notch for notch operation and filter1_bpf for high frequency noise removal filter. The binary coefficients are generated and the filter coefficients are stored in the FIR input package. Filter2_notch for notch operation. The package is created which consists

of the filter coefficients and will be called into the program. The FIR structure is shown in the below fig. 5.7 Input is taken as FIR input and is given to the multiplier in a loop and another input to multiplier is the filter coefficients (n) stored in the FIR input package. Result generated by the multiplier will be added with another multiplier in the loop (n+1).Loop will be running until last coefficient is multiplied and result is reflected on the output signal filter o/p.

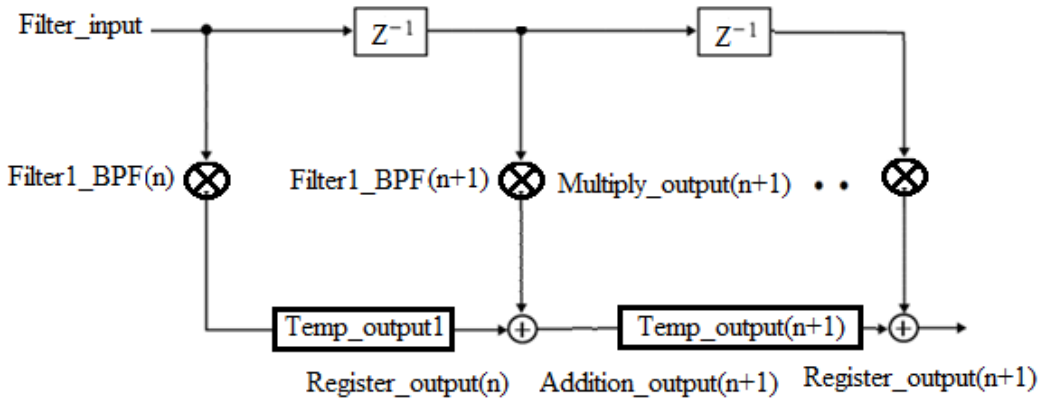


Fig. 5.7 FIR filter implementation

5.2 'R' Peak Detection in ECG Signal

The major problem associated with the analysis of ECG signal is the accurate detection of the R-peaks. It is difficult since it is varying with time, the physiological changes due to the patient and the added noise. The noise includes the movement of the patient while performing ECG, poor connectivity of the electrodes, muscle contraction interference, power line noise and the base line wandering due to respiration. The applications of R peaks require the accurate HRV which includes the ICU units in hospitals, implantable pacemakers, operating rooms and defibrillators.

The methodology of R peak detection of ECG signal is proposed since it is adaptive to the non-linear and time dependent features of the signal. The steps are used to recognize the normal waveform and removes the unwanted artic rafts and noise.

The R peaks, which are the part of QRS complex[76], will improve the multiple features, has 'RR' interval, duration of the pulse and the amplitude of the signal. The irregular distance between the peaks is required for the processing of ECG \, present of low frequency components in the ECG, which includes due to patient breathing, uneven peak form, are heart diseases are to be estimated. The frequency domain analysis of ECG signal is required to justify the application in quantitative ECG, for the accurate detection of R peaks and its shape is same as the QRS complex. The R peak is the most vital part of an Electrocardiogram signal analysis, which is corresponding to the ventricles part in the heart during heartbeat. The fig. 5.8 is used for detecting the R peaks from the noise corrupted ECG signal.

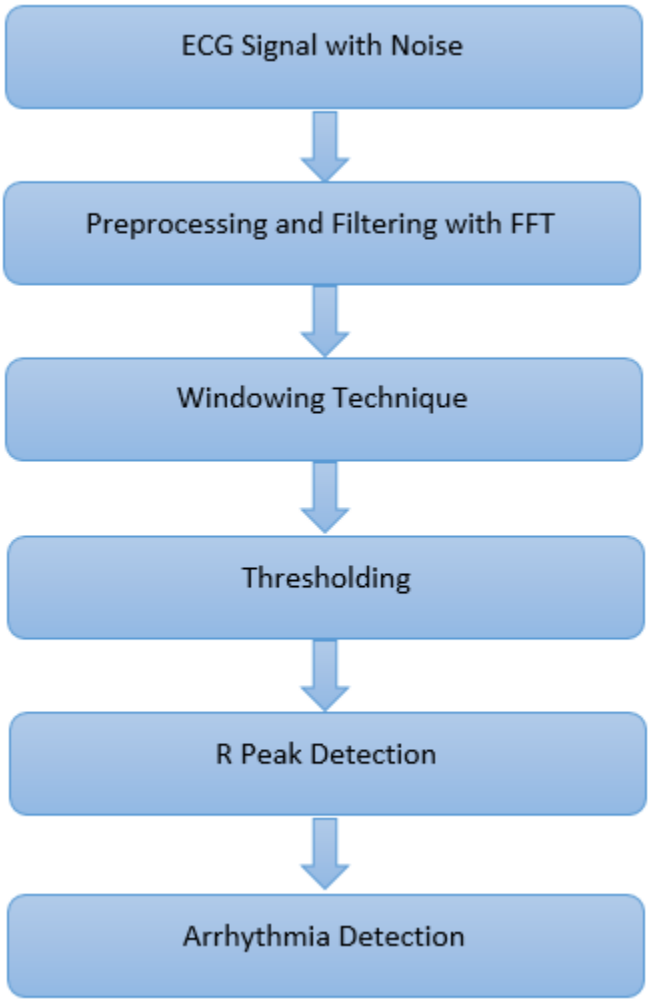


Fig. 5.8 R- Peak Detection in ECG

ECG signal with noise is the the sampled data from the MIT-BIH database [67] the ECG samples are added with the noise and the sampling frequency is 1kHz and the duratin of the ECG signal is of 10 minutes length and which is not uniform. To make the signal uniformity the low frequency components 45 Hz should be removed by the Fast Fourier transform technique.The second block includes the FFT and IFFT to get back the original time domain samples.The third block is about the windowing technique which is used to find the maximum value with the default window size of 512 and the next step is the thresholding which uses to detain the small peaks from the ECG signal and to preserve the significant ones The next step is to overlap the noisy signal with the R peaks after getting the R -peaks from the noisy ECG signal and the average of the peaks is taken to calculate the heart beat for the dissimilar test cases. Cardiac arrythima tells the condition of the patient a slow heart rate or the fast heart rate by using the heart rate [70] equation which is given below.

$$Heart\ Rate = \left(\frac{Sampling\ Rate}{RR\ Interval\ in\ Samples}\right) \times 60 \qquad (5.3)$$

5.3 MATLAB Simulation ECG signal

THE MATLAB simulation is carried out using signal-processing tool. The steps of patient-1 simulation is listed below.

5.3.1 ECG data

Step 1: ECG sampled data is taken from the MIT-BIH database and Fast Fourier transform technique is applied. The original ECG signal P_n from the body of the patient $P_n = P_1, P_2, P_3, P_4 \ldots\ldots\ldots\ldots P_N$. Where n = 1, 2, 3…….N and N is the length of the input signal shown in fig. 5.9.The length of the input is taken as 17000 samples, sampling frequency is 1000 Hz., 10 minutes of data is captured. The captured input data is compatible with MATLAB. By closely observing the zoomed

input signal of the ECG signal. Fig. 5.10 shows the zoomed ECG signal contaminated with the several noises.

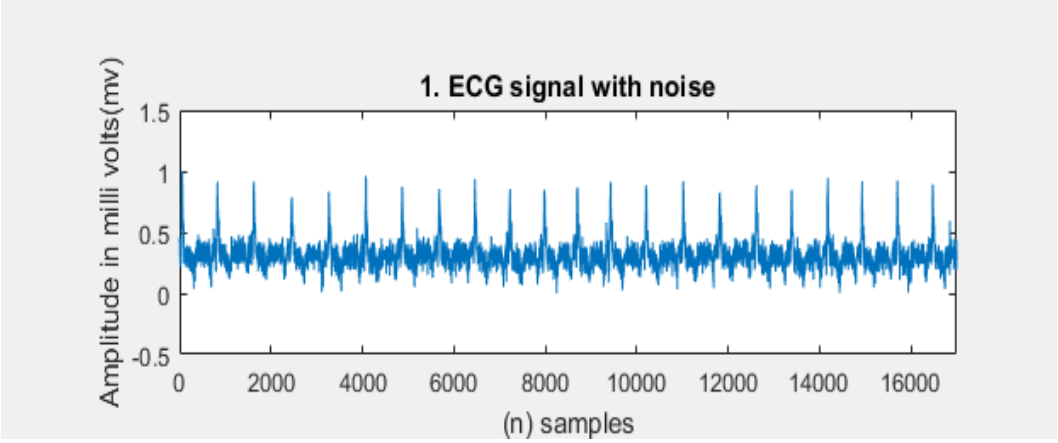


Fig. 5.9 Original ECG signal added with noise

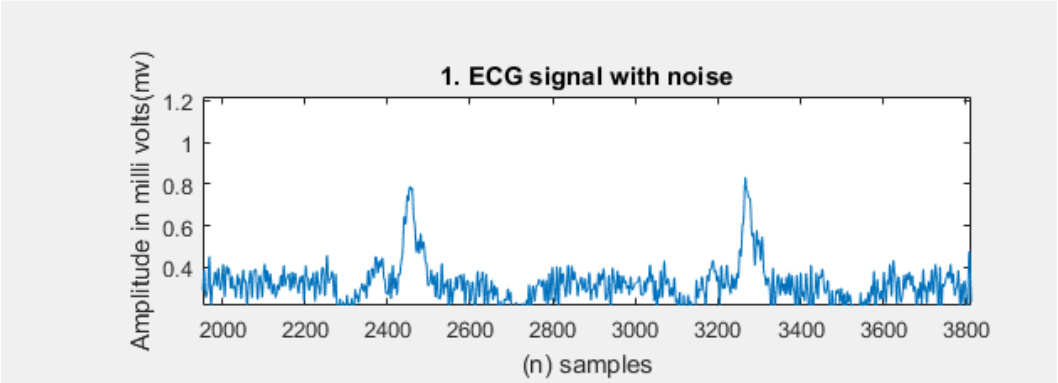


Fig. 5.10 Zoomed ECG signal with noise

The graph shown in Fig.5.11 is not uniformly distributed. That's what first step of the algorithm is to straighten it. In order to straighten it all the low frequency components should be removed. The X-axis values represent samples and the Y-axis represents the voltage in milli volts. Apply the Fast Fourier transform-FFT to the ECG signal using Equation (5.4)

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{\frac{-j2\pi nk}{N}} \qquad Where, K = 0,1,2,\ldots..N-1 \qquad (5.4)(84)$$

The FFT is applied to the 16384 samples to remove the low frequency components and to retain the remaining samples. Again, IFFT is applied to the signal to get back the original time domain signal.

$$X(n) = \frac{1}{N}\sum_{k=0}^{N-1} x(k)e^{\frac{j2\pi nk}{N}} \qquad Where, \qquad n = 0,1,2,\ldots..k-1 \qquad (5.5)$$

Equation (5.4) removes low frequencies by using FIR filter and restore ECG with the help of IFFT (5.5). The simulation, which includes the FFT and IFFT, is shown in fig. 5.11.

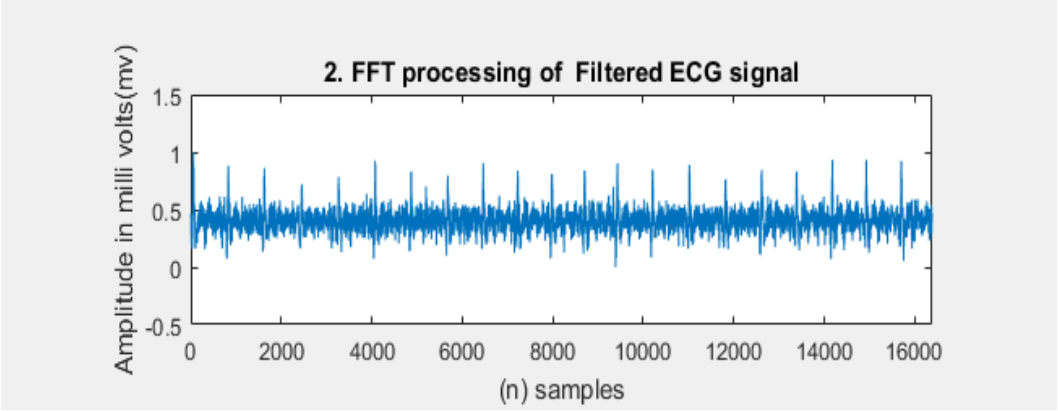


Fig. 5.11 FFT processing of ECG signal

The process of removing the lower frequencies and considering only the QRS waves which have relatively larger frequencies as compared to the remaining like P, T and U waves.

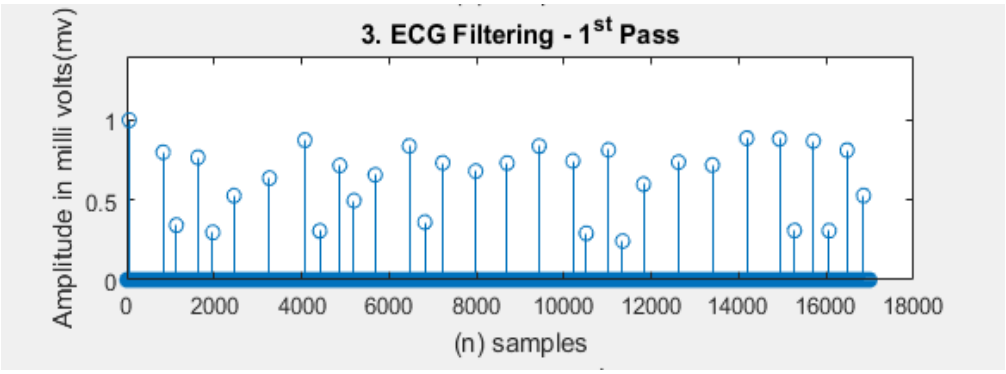


Fig. 5.12 Filtered ECG-1st pass.

Step 2: Using a windowing filter. Second step is to find local maxima that observe only maximum in the window. The window size is taken as the default window size that is 571.Which means that the peak is detected for every 571 samples and ignore the others.

Step 3: After the step of windowing filter, apply the threshold filter to remove the small peaks and preserve the significant ones. The graph after applying the threshold filter appears as in Fig. 5.13.

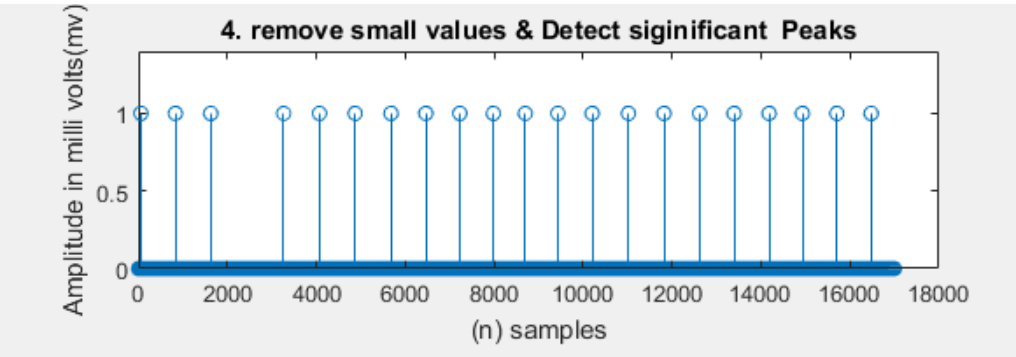


Fig. 5.13 Detected peaks.

5.3.2 Adjusted Filter

The simulation results in fig.5.13 is satisfying the conditions of detected peaks but do not assure that all the peaks are normal. To overcome this, the size of the filter window is altered and filtering techniques are repeated to estimate the peaks as shown in Fig. 5.14 with the help of adjusted filter as second time filtering. The quality of graph is more desirable than Fig. 5.13.

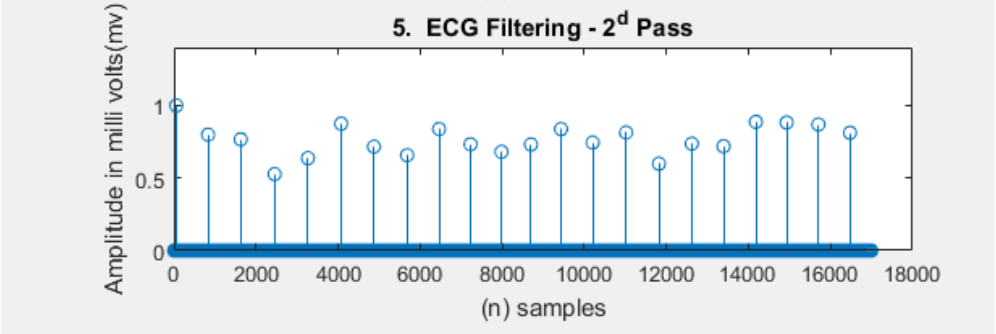


Fig. 5.14 Filtered ECG - Second pass.

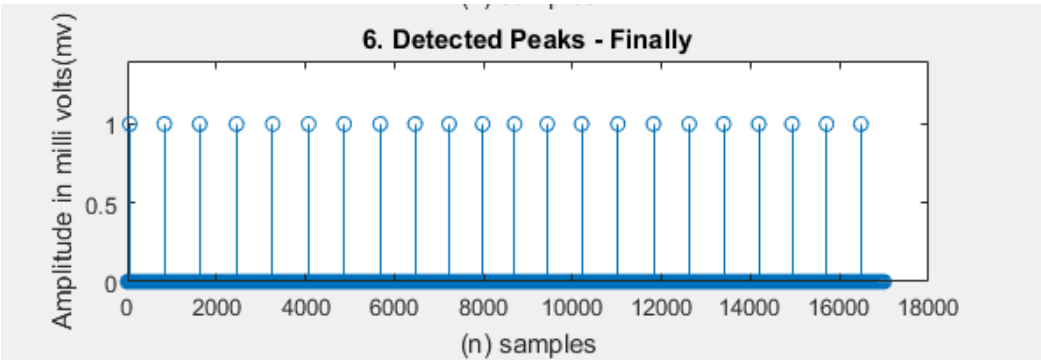


Fig. 5.15 Final detected peaks.

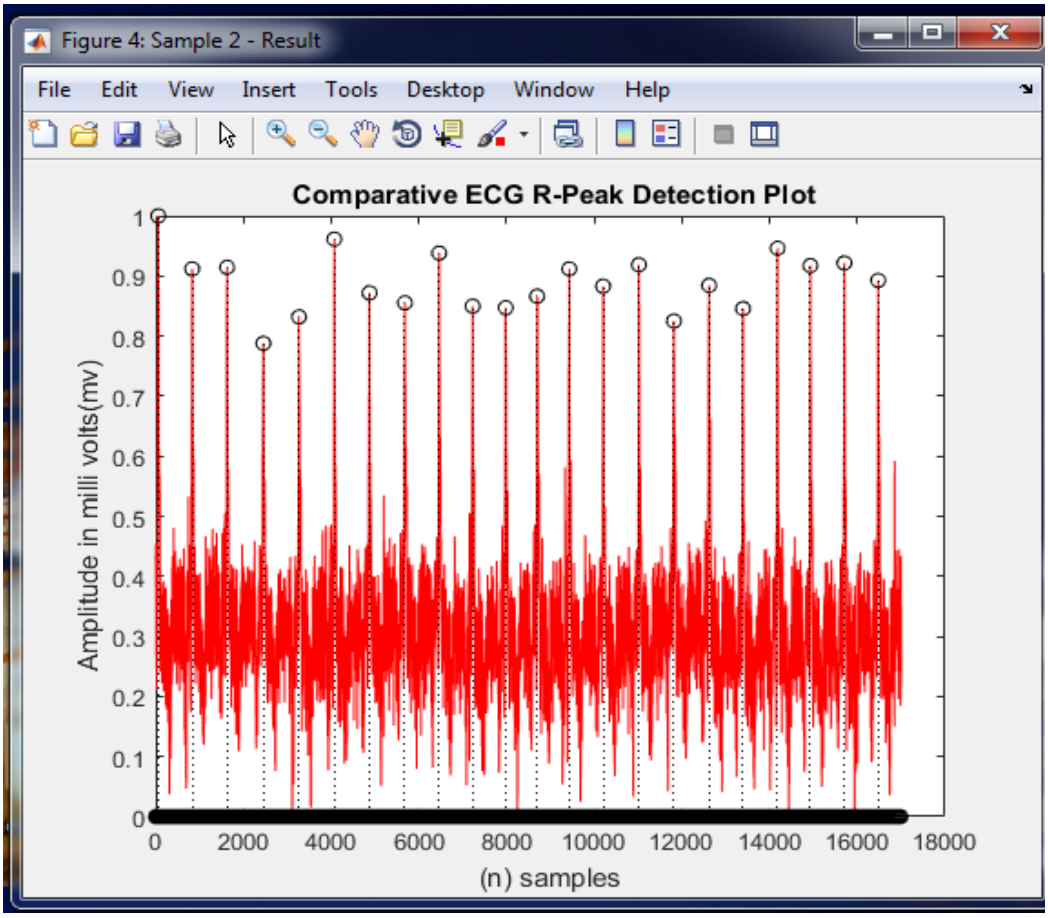


Fig. 5.16 ECG R-peak detection plot

The resultant peaks are depicted in shown in Fig. 5.15. The Fig. 5.16 shows the overlapped R peaks with the ECG signal associated with the noise, used for the heart rate calculation (BPM).

5.4 Heart Rate Calculation

The number of times a heart beats per minute is heart rate. For a normal person, heart beats 60 to 100 times per minute so the normal value is 60 to 100 beats per minute. If the heart rate is slower, and then the condition is called Bradycardia. If the heart rate is higher, then it is tachycardia and unevenly spaced cycles specify an arrhythmia [85]. If PR interval is more than 0.2 Sec, blockage of AV node is indicated. The equation to calculate heart rate calculation is followed to calculate the heart beat.

5.4.1 Bradycardia

The heart beats less than 60 BPM [85] then it is slower heart rate. This condition can be observed in athletes and the patients suffering from jaundice, myxedema and in patients with increased intra carinal pressure.

5.4.2 Tachycardia

The heart rate is greater than 100 BPM, it is tachycardia. Atrium having ectopic focus that regularly beats at a higher rate causes tachycardia.

5.4.3 Beats per Minute (BPM)

The 30 patient's ECG samples are taken from physionet.org website [38] and the R-peak detection technique is executed. The technique optimizes the processing time besides the accuracy of the detection. The heart beat calculations follows all the steps discussed in Fig. 5.9 to Fig. 5.16 to check the cardiac arrhythmia. The simulation steps are carried out sequentially and calculated BPM for normal case is 67.The average 'R-R' interval is the distance between the first peak and the last peak divided by the total number of peaks from fig. 5.16. The first peak is considered as P_X and the last peak is considered as P_y. Total number of peaks are P_T then "R-R" interval is given by equ.(5.6)

$$RR = \left(\frac{P_y - P_x}{P_T}\right) \quad samples \qquad (5.6)$$

After calculating the “R-R” interval, the next step is to find the average heart rate by substituting the value of “R-R” interval.

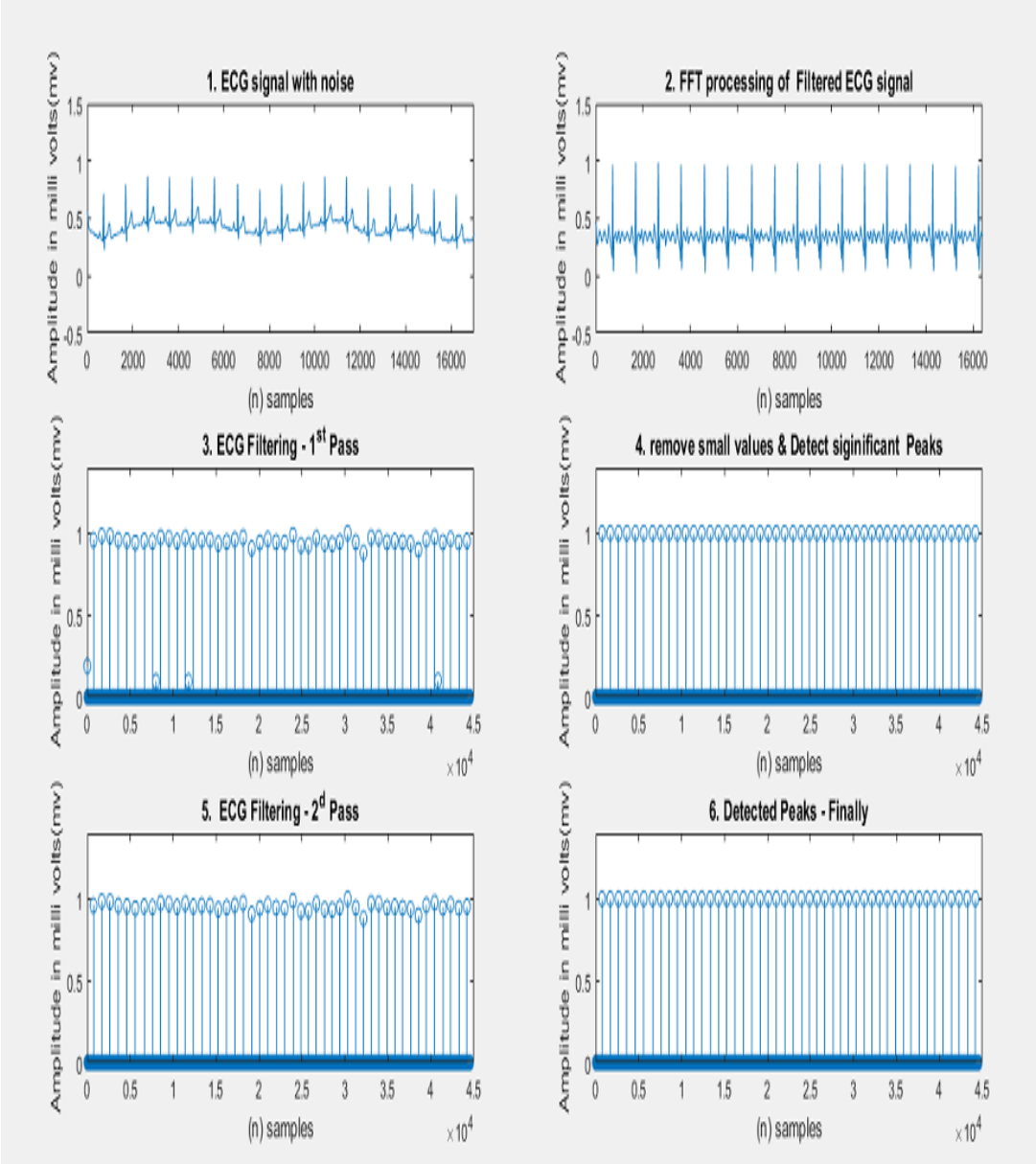


Fig. 5.17 MATLAB Simulation Steps for (Patient-2)

The patient-1 simulation results provides P_y = 16000 and P_X = 4 and P_T = 19. Substituting the values in equation (5.6), the RR interval value is 895 samples and further calculated heart rate value is 67 with respect to sampling rate of 1000 Hz.

$$RR = \left(\frac{P_y - P_x}{P_T}\right) = \left(\frac{16000 - 4}{19}\right) = 895\ samples$$

$$Heart\ Rate = \left(\frac{Sampling\ Rate}{RR\ Interval\ in\ Samples}\right) \times 60 = \left(\frac{1000}{895}\right) \times 60 = 67$$

The same procedure is carried out for the ECG data of patient-2 taken from physionet.org website [38]. The simulation steps are shown in fig. 5.17 and resultant RR peak simulation in fig. 5.18 to estimate the values of P_y, P_X and P_T.

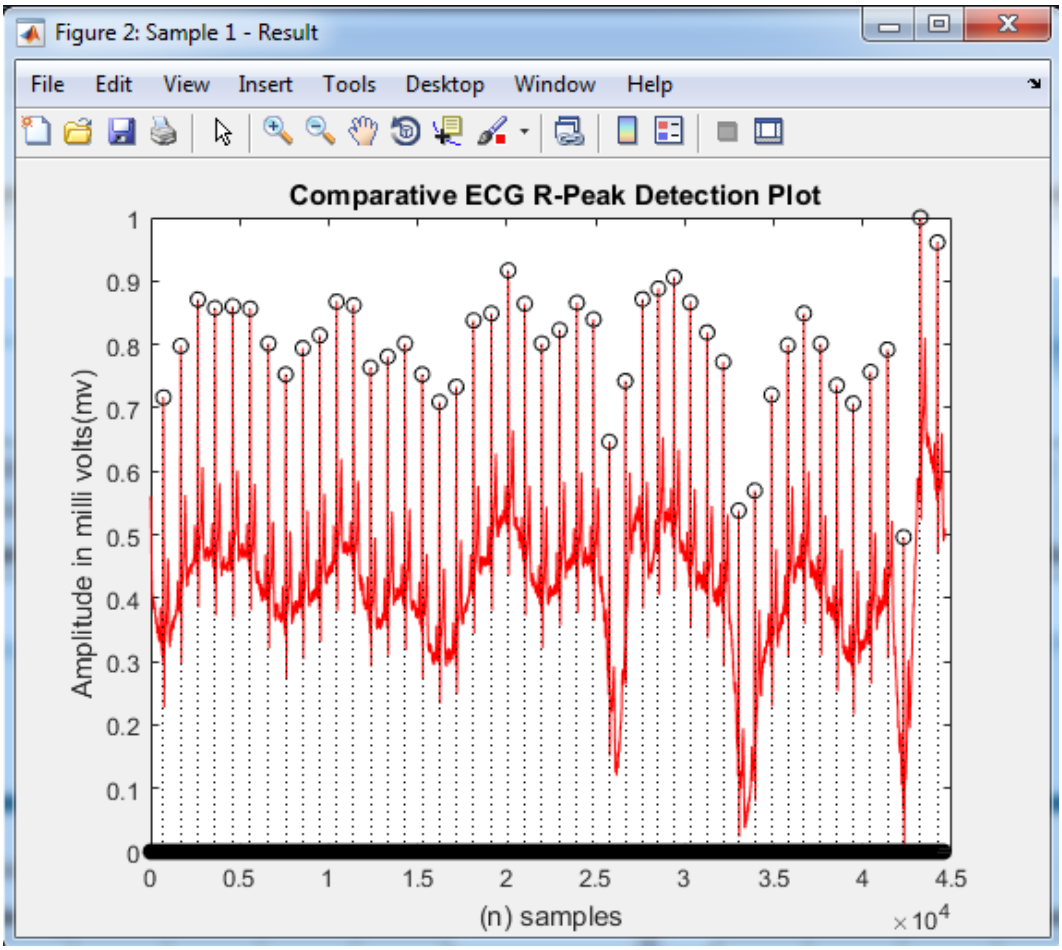


Fig. 5.18 ECG R- Peak Detection Plot (Patient-2)

The patient-2 simulation results provides P_y = 25680 and P_X = 3 and P_T = 48. Substituting the values in equation (5.6), the RR interval value is 535 samples and further calculated heart rate value is 67 with respect to sampling rate of 1000 Hz.

$$RR = \left(\frac{P_y - P_x}{P_T}\right) = \left(\frac{25680 - 3}{48}\right) = 535\ samples$$

$$Heart\ Rate = \left(\frac{Sampling\ Rate}{RR\ Interval\ in\ Samples}\right) \times 60 = \left(\frac{1000}{535}\right) \times 60 = 112$$

In the same way the simulation is carried over for 30 patients. Table 5.1 shows the cacluation of RR peaks and heart rate calclutions to estimate estimate the patient is Normal, Bradycardia and Tachycardia. Table 5.2 shows the heart rate with Normal (60-100 BPM), Bradycardia (< 60) and Tachycardia (> 100) conditions to estimate the patient heart status.

Table 5.1 Calculations of RR peaks and heartbeat of patients

S. No	Simulated Values	$RR = \left(\frac{P_y - P_x}{P_T}\right)$	Heart Rate $= \left(\frac{Sampling\ Rate}{RR\ Interval\ in\ Samples}\right) \times 60$
Patient-1	$P_X = 4$ $P_y = 16000$ $P_T = 19.$	$\left(\frac{16000 - 4}{19}\right) = 895$	$\left(\frac{1000}{895}\right) \times 60 = 67$
Patient-2	$P_X = 3$ $P_y = 25560$ $P_T = 48.$	$\left(\frac{25860 - 3}{48}\right) = 535$	$\left(\frac{1000}{535}\right) \times 60 = 112$
Patient-3	$P_X = 7$ $P_y = 17493$ $P_T = 21.$	$\left(\frac{17493 - 7}{21}\right) = 832$	$\left(\frac{1000}{832}\right) \times 60 = 72$
Patient-4	$P_X = 9$ $P_y = 45271$ $P_T = 40.$	$\left(\frac{45271 - 9}{40}\right) = 1132$	$\left(\frac{1000}{1132}\right) \times 60 = 53$
Patient-5	$P_X = 7$ $P_y = 13592$ $P_T = 17.$	$\left(\frac{13592 - 7}{17}\right) = 800$	$\left(\frac{1000}{800}\right) \times 60 = 75$

Patient-6	$P_X = 8$ $P_y = 12504$ $P_T = 24.$	$\left(\frac{12504-8}{24}\right) = 521$	$\left(\frac{1000}{521}\right) \times 60 = 115$
Patient-7	$P_X = 8$ $P_y = 16926$ $P_T = 22.$	$\left(\frac{16926-8}{22}\right) = 769$	$\left(\frac{1000}{769}\right) \times 60 = 78$
Patient-8	$P_X = 4$ $P_y = 22138$ $P_T = 31.$	$\left(\frac{22138-4}{31}\right) = 714$	$\left(\frac{1000}{714}\right) \times 60 = 84$
Patient-9	$P_X = 9$ $P_y = 15003$ $P_T = 14.$	$\left(\frac{15003-9}{14}\right) = 1071$	$\left(\frac{1000}{1071}\right) \times 60 = 56$
Patient-10	$P_X = 7$ $P_y = 17647$ $P_T = 20.$	$\left(\frac{17647-7}{20}\right) = 882$	$\left(\frac{1000}{882}\right) \times 60 = 68$
Patient-11	$P_X = 8$ $P_y = 16926$ $P_T = 22.$	$\left(\frac{16926-8}{22}\right) = 769$	$\left(\frac{1000}{769}\right) \times 60 = 71$
Patient-12	$P_X = 5$ $P_y = 20105$ $P_T = 30.$	$\left(\frac{20105-5}{30}\right) = 667$	$\left(\frac{1000}{667}\right) \times 60 = 90$
Patient-13	$P_X = 3$ $P_y = 16280$ $P_T = 19.$	$\left(\frac{16280-3}{19}\right) = 857$	$\left(\frac{1000}{857}\right) \times 60 = 70$
Patient-14	$P_X = 9$ $P_y = 12361$ $P_T = 14.$	$\left(\frac{12361-9}{14}\right) = 882$	$\left(\frac{1000}{882}\right) \times 60 = 68$
Patient-15	$P_X = 4$ $P_y = 16684$ $P_T = 15.$	$\left(\frac{16684-4}{15}\right) = 1112$	$\left(\frac{1000}{1112}\right) \times 60 = 54$

Patient-16	$P_X = 9$ $P_y = 8409$ $P_T = 14.$	$\left(\frac{8409-9}{14}\right) = 600$	$\left(\frac{1000}{600}\right) \times 60 = 100$
Patient-17	$P_X = 5$ $P_y = 17276$ $P_T = 19.$	$\left(\frac{17276-5}{19}\right) = 909$	$\left(\frac{1000}{909}\right) \times 60 = 66$
Patient-18	$P_X = 8$ $P_y = 17501$ $P_T = 21.$	$\left(\frac{17501-8}{21}\right) = 833$	$\left(\frac{1000}{833}\right) \times 60 = 72$
Patient-19	$P_X = 6$ $P_y = 12187$ $P_T = 13.$	$\left(\frac{12187-6}{13}\right) = 937$	$\left(\frac{1000}{937}\right) \times 60 = 64$
Patient-20	$P_X = 6$ $P_y = 15888$ $P_T = 18.$	$\left(\frac{15888-6}{18}\right) = 882$	$\left(\frac{1000}{882}\right) \times 60 = 68$
Patient-21	$P_X = 7$ $P_y = 23667$ $P_T = 28.$	$\left(\frac{23667-7}{28}\right) = 845$	$\left(\frac{1000}{845}\right) \times 60 = 71$
Patient-22	$P_X = 4$ $P_y = 15733$ $P_T = 16.$	$\left(\frac{15733-4}{16}\right) = 983$	$\left(\frac{1000}{983}\right) \times 60 = 61$
Patient-23	PX = 5 Py=16620 PT = 18.	$\left(\frac{16620-5}{18}\right) = 923$	$\left(\frac{1000}{923}\right) \times 60 = 65$
Patient-24	$P_X = 9$ $P_y = 13451$ $P_T = 13.$	$\left(\frac{13451-9}{13}\right) = 1034$	$\left(\frac{1000}{1034}\right) \times 60 = 58$
Patient-25	$P_X = 4$ $P_y = 20860$ $P_T = 24.$	$\left(\frac{20860-4}{24}\right) = 869$	$\left(\frac{1000}{869}\right) \times 60 = 69$

Patient-26	$P_X = 6$ $P_y = 18470$ $P_T = 32.$	$\left(\frac{18470-6}{32}\right) = 577$	$\left(\frac{1000}{577}\right) \times 60 = 104$
Patient-27	$P_X = 8$ $P_y = 16370$ $P_T = 18.$	$\left(\frac{16370-8}{18}\right) = 909$	$\left(\frac{1000}{909}\right) \times 60 = 66$
Patient-28	$P_X = 5$ $P_y = 18653$ $P_T = 23.$	$\left(\frac{18653-5}{23}\right) = 811$	$\left(\frac{1000}{811}\right) \times 60 = 74$
Patient-29	$P_X = 9$ $P_y = 10149$ $P_T = 12.$	$\left(\frac{10149-9}{12}\right) = 845$	$\left(\frac{1000}{845}\right) \times 60 = 71$
Patient-30	$P_X = 8$ $P_y = 16577$ $P_T = 21.$	$\left(\frac{16577-8}{21}\right) = 789$	$\left(\frac{1000}{789}\right) \times 60 = 76$

Table 5.2 Heart rate with patient status

S. No.	**ECG sample collected from physionet.org database**	**Heart rate**	**Patient Heart Status**
Patient-1	Record ptbdb/patient001/s0014lre from 0:00.000 to 1:00.000	67	Normal
Patient-2	Record ptbdb/patient003/s0017lre from 0:00.000 to 1:00.000	112	Tachycardia
Patient-3	Record ptbdb/patient007/s0026lre (i) , from 0:00.000 to 1:00.000	72	Normal
Patient-4	Record ptbdb/patient035/s0145lre (ii) from 0:00.000 to 1:00.000	53	Bradycardia

Patient-5	Record ptbdb/patient067/s0230lre (iii) , from 0:00.000 to 1:00.000	75	Normal
Patient-6	Record ptbdb/patient180/s0545_re (avr) , from 0:00.000 to 1:00.000	115	Tachycardia
Patient-7	Record ptbdb/patient219/s0441_re (avr) , from 0:00.000 to 1:00.000	78	Normal
Patient-8	Record ptbdb/patient286/s0546_re , from 0:00.000 to 1:00.000	84	Normal
Patient-9	Record ptbdb/patient289/s0550_re , from 0:00.000 to 1:00.000	56	Bradycardia
Patient-10	Record ptbdb/patient294/s0559_re , from 0:00.000 to 1:00.000	68	Normal
Patient-11	record ptbdb/patient008/s0068lre , from 0:00.000 to 0:10.000record	71	Normal
Patient-12	Record ptbdb/patient009/s0035_re , from 0:00.000 to 0:10.000	90	Normal
Patient-13	Record ptbdb/patient010/s0036lre , from 0:00.000 to 0:10.000	70	Normal
Patient-14	Record ptbdb/patient011/s0049lre , from 0:00.000 to 0:10.000	68	Normal
Patient-15	Record ptbdb/patient012/s0050lre , from 0:00.000 to 0:10.000	54	Bradycardia
Patient-16	Record ptbdb/patient013/s0072lre , from 0:00.000 to 1:00.000	100	Normal
Patient-17	Record ptbdb/patient014/s0071lre , from 0:00.000 to 1:00.000	66	Normal
Patient-18	Record ptbdb/patient015/s0057lre , from 0:00.000 to 1:00.000	72	Normal
Patient-19	Record ptbdb/patient020/s0079lre , from 0:00.000 to 1:00.000	64	Normal

Patient-20	Record ptbdb/patient024/s0084lre , from 0:00.000 to 1:00.000	68	Normal
Patient-21	Record ptbdb/patient028/s0090lre , from 0:00.000 to 1:00.000	71	Normal
Patient-22	Record ptbdb/patient040/s0131lre , from 0:00.000 to 1:00.000	61	Normal
Patient-23	Record ptbdb/patient050/s0215lre , from 0:00.000 to 1:00.000	65	Normal
Patient-24	Record ptbdb/patient055/s0194lre , from 0:00.000 to 1:00.000	58	Bradycardia
Patient-25	Record ptbdb/patient065/s0229lre , from 0:00.000 to 1:00.000	69	Normal
Patient-26	Record ptbdb/patient070/s0235lre , from 0:00.000 to 1:00.000	104	Tachycardia
Patient-27	Record ptbdb/patient073/s0252lre , from 0:00.000 to 1:00.000	66	Normal
Patient-28	Record ptbdb/patient080/s0261lre , from 0:00.000 to 1:00.000	74	Normal
Patient-29	Record ptbdb/patient105/s0303lre , from 0:00.000 to 1:00.000	71	Normal
Patient-30	Record ptbdb/patient215/s0437_re , from 0:00.000 to 0:10.000	78	Normal

Fig. 5.19 shows the graph for RR intervals carried for patient-1 to patient- 30. In the same way fig. 5.20 shows the graph for heart rate corresponding to patient-1 to patient- 30.

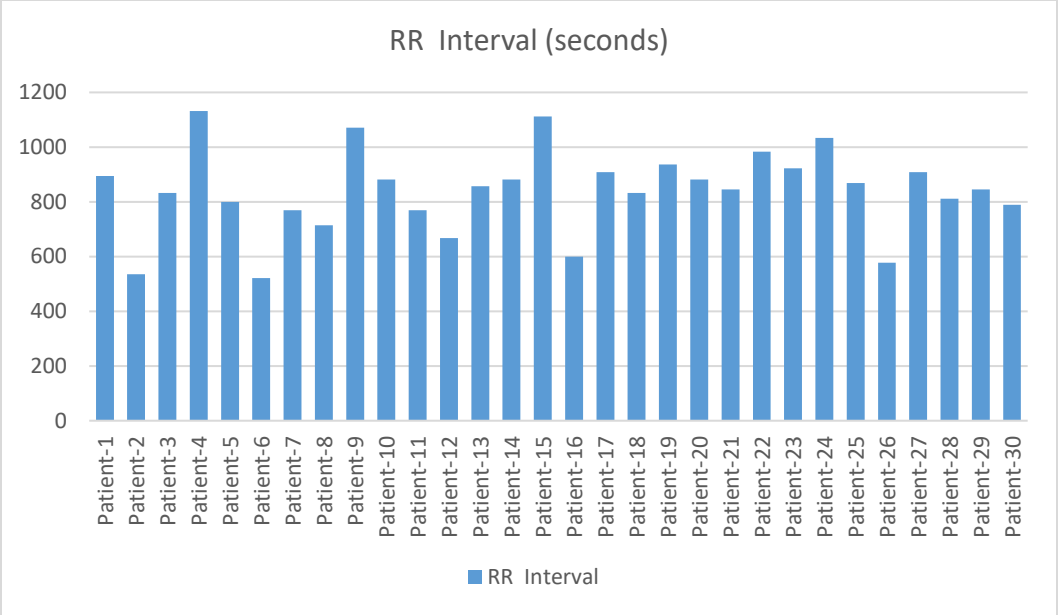


Fig. 5.19 RR intervals corresponding to 30 patients

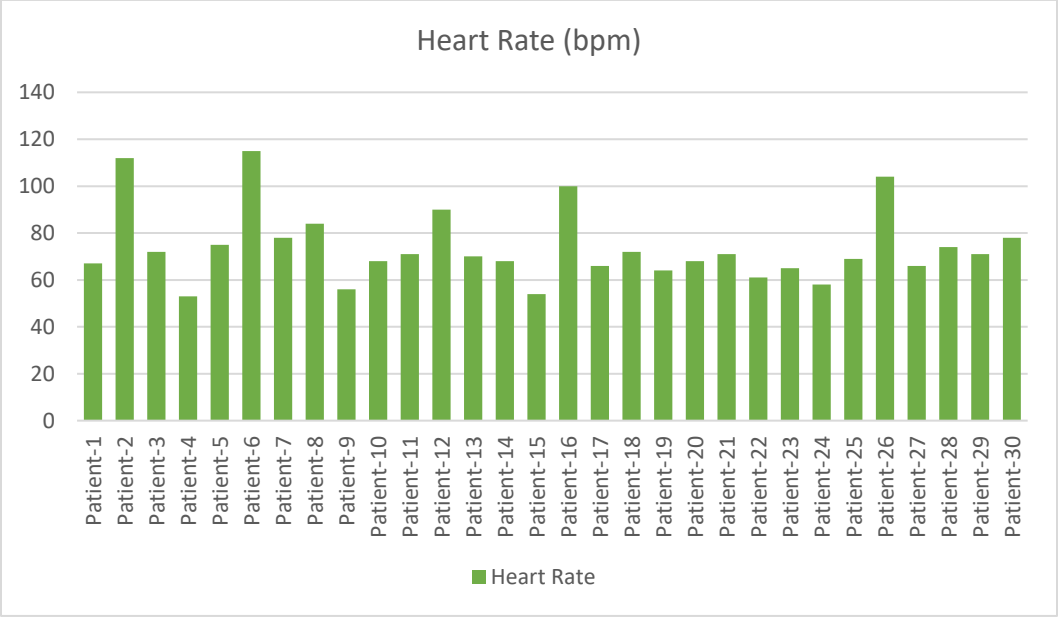


Fig. 5.20 Heart rate values of 30 patients

5.5 Statistical Analysis

The analysis of the heart rate is done based on the 'z' statistics test. Table 5.3 Calculation for the statistical analysis of the heart rate using 'z' test. The equation used of to calculate the value of 'z' is given as

$$z = \frac{\bar{X} - \mu_{H0}}{SE} = \frac{X - \mu_{H0}}{\sigma_p/\sqrt{n}} \quad (5.7)$$

Where,

$$\sigma_p = \sqrt{\frac{\sum(X_i - \bar{X})^2}{n}} \quad (5.8)$$

$$\bar{X} = \frac{x_1 + x_2 \ldots\ldots\ldots\ldots\ldots x_n}{n} \quad (5.9)$$

Here, $\bar{X}$ = μ = mean of sample

μ_{H0} = mean of the population

σ_p = standard deviation of the population

n = no. of observations

Let us assume that null hypothesis $H_0 = \mu_{H0} = 72$ and

Alternate Hypothesis $H_a = \mu_{H0} \neq 72$

Table 5.3 Calculation for the statistical analysis of the heart rate

S. No.	$\mathbf{X_i}$	$(\boldsymbol{X_i - \bar{X}})$	$(\boldsymbol{X_i - \bar{X}})^2$
Patient-1	67	-5	25
Patient-2	112	40	1600
Patient-3	72	0	0
Patient-4	53	-19	361
Patient-5	75	3	9
Patient-6	115	43	1849
Patient-7	78	6	36

Patient-8	84	12	144
Patient-9	56	-16	256
Patient-10	68	-4	16
Patient-11	71	-1	1
Patient-12	90	18	324
Patient-13	70	-2	4
Patient-14	68	-4	16
Patient-15	54	-18	324
Patient-16	100	28	784
Patient-17	66	-6	36
Patient-18	72	0	0
Patient-19	64	-8	64
Patient-20	68	-4	16
Patient-21	71	-1	1
Patient-22	61	-11	121
Patient-23	65	-7	49
Patient-24	58	-14	196
Patient-25	69	-3	9
Patient-26	104	32	1024
Patient-27	66	-6	36
Patient-28	74	2	4
Patient-29	71	-1	1
Patient-30	78	6	36
	$\boldsymbol{\bar{X} = 74}$	$\boldsymbol{\sum(X_i - \bar{X}) = 60}$	$\boldsymbol{\sum(X_i - \bar{X})^2 = 7342}$

$$\sigma_p = \sqrt{\frac{\sum(X_i - \bar{X})^2}{n}} = \sqrt{\frac{7342}{30}} = 15.73$$

Standard Error,

$$SE = \frac{\sigma_p}{\sqrt{n}} = \frac{15.73}{\sqrt{30}} = 2.87$$

$$z = \frac{\bar{X} - \mu_{H0}}{SE} = \frac{(74 - 72)}{2.87} = \frac{2}{2.87} = 0.696$$

The value of z is 0.696 and applying the two-tailed test for determining the rejection regions at 5 % level of significance, which comes to under using normal curve followed for Z area table

$$R: |z| > 1.96$$

Hence, our hypothesis $H_0 = \mu_{H0} = 72$ is accepted to estimate that the mean is consistent with the population mean and population mean is supporting to our results. The value $z = 0.696$ provides the positive results to support our MATLAB simulation.

CHAPTER 6

RESULTS AND DISCUSSIONS

The chapter details the all simulation and design outcomes as main results with respect to designed ADC module, high frequency noise removal FIR filter module, ECG- ROM module, FFT module as STFT, magnitude calculation module and top-level ECG System chip. The hardware design summary and timing parameters are also discussed with Virtex 5, synthesis process, analysis and verification in Xilinx 14.2 ISE and Modelsim software.

6.1 Xilinx and Modelsim Simulation of ADC

The ECG system chip consist of the ADC module, ADC interface module, high frequency noise removal FIR filter module, ECG- ROM module, 1024 FFT module as STFT, magnitude calculation module.

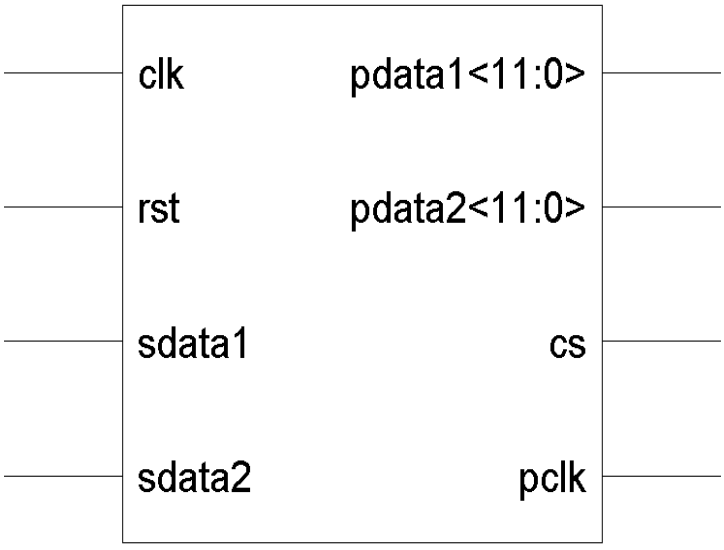


Fig. 6.1 RTL view of PMOD ADC

The RTL of PMoD ADC is shown in fig. 6.1 and its internal schematic is shown in fig. 6.2. The RTL shows the all posible inputs and outputs of the developed chip with size of each pin. Internal schemtic shows the internal circuitry having the internal hardware with combonation cricuits such as gate, adders, substractors and sequnetial circuits sich as flip flops, regsiters, latches etc. The detail of the pins corresponmding to ADC module and interface logic is listed in table 6.1.

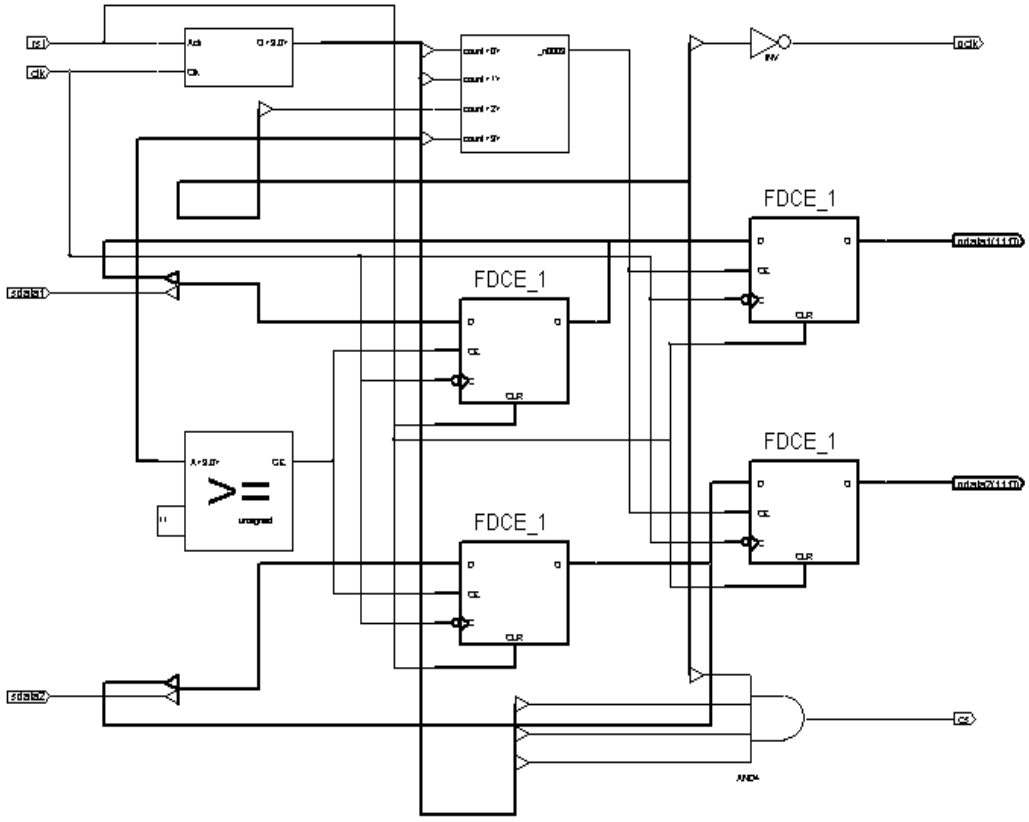


Fig. 6.2 Internnal schematic of PMOD ADC

Table 6.1 Pin details of PMOD ADC chip

Pin	**Direction**	**Detail**
clk(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation we are giving 50 % duty cycle clock signal

rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clock signal
sdata1(1 bit)	Input	It is the first input port data of 1 bit for 16 bit input value of ADC chip coming 1 bit sequentially based on successive approximation techniques as ‘0’ and ‘1’
sdata2(1 bit)	Input	It is the second input port data of 1 bit for 16 bit input value of ADC chip coming 1 bit sequentially on rising edge of clk.
cs(1 bit)	Output	It is the flag output to indicate that 16 bit input is taken with respect to count values. When count = 15 then the data in shift register will be reflected parallel on to pdata2(12 bit data) .At this time cs will be active high signal.
pclk(1 bit)	Output	It is the active Input/output signal and associated with clk. When count = 8, the signal will high.
pdata1(11:0) (12 bit)	Output	It is 12 bit parallel output data corresponding to serial data1 (sdata1)
pdata2(11:0) (12 bit)	Output	It is 12 bit parallel output data corresponding to serial data2 (sdata2)

The Modelsim simulation waveform for PMOD- ADC chip is shown in fig. 6.3. In the simulation process,

Step-1: Force reset = ‘1’ in software then count, pdata1 (11:0) and pdata2 (11:0) will be zero.

Step 2 : Force reset = ‘0’, apply direct clk signal with rising edge, sdata1 = ‘1’ and sdata2 = ‘0’, then the output will appear on pdata1= “111111111111”, pdata2= “0000000000”, and CS = ‘1’.

Step 3 : Force reset = ‘0’, apply direct clk signal with rising edge, sdata1 = ‘0’ and sdata2 = ‘1’, then the output will appear on pdata1 = “0000000000”, pdata2= “111111111111”, and CS = ‘1’.

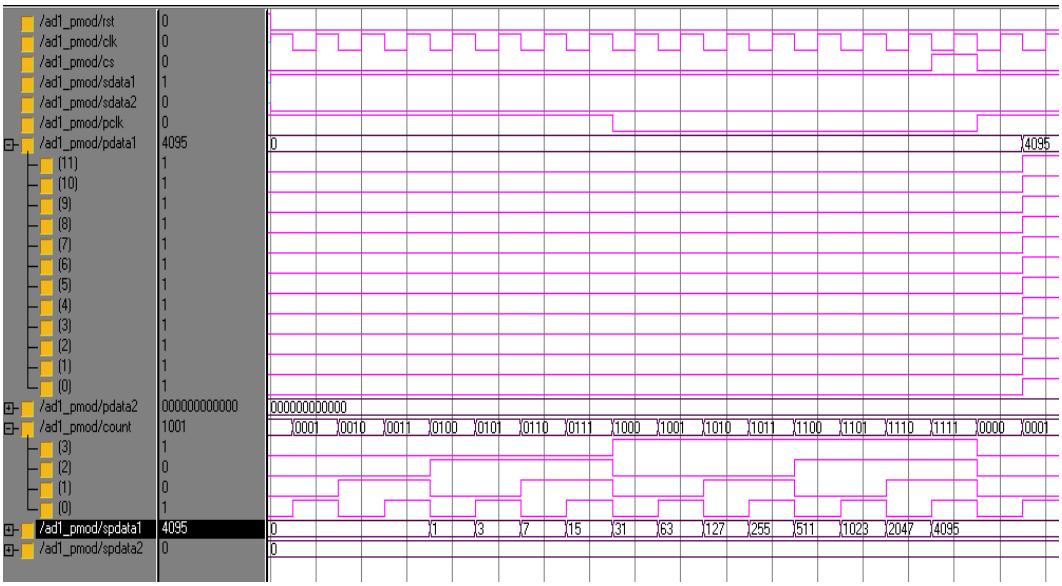


Fig. 6.3 Modelsim simulation of PMOD ADC

6.2 Xilinx and Modelsim Simulation of FIR Filter

The RTL view and internal schematic of high frequency noise removal FIR filter module is presented in fig. 6.4 and fig. 6.5 respectively. The pin details of the filter chip is given in table 6.2.

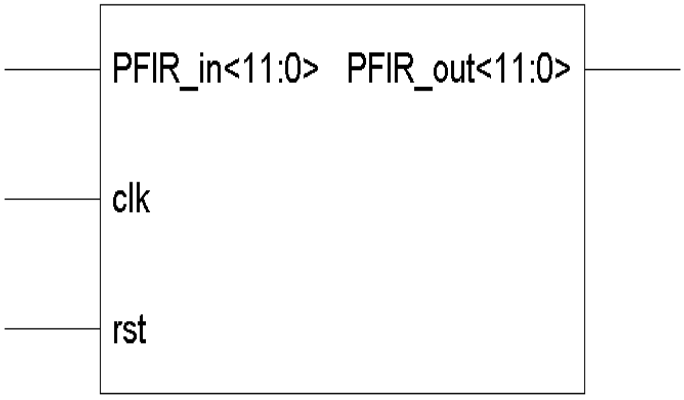


Fig. 6.4 RTL View of High Frequency Noise Removal FIR filter

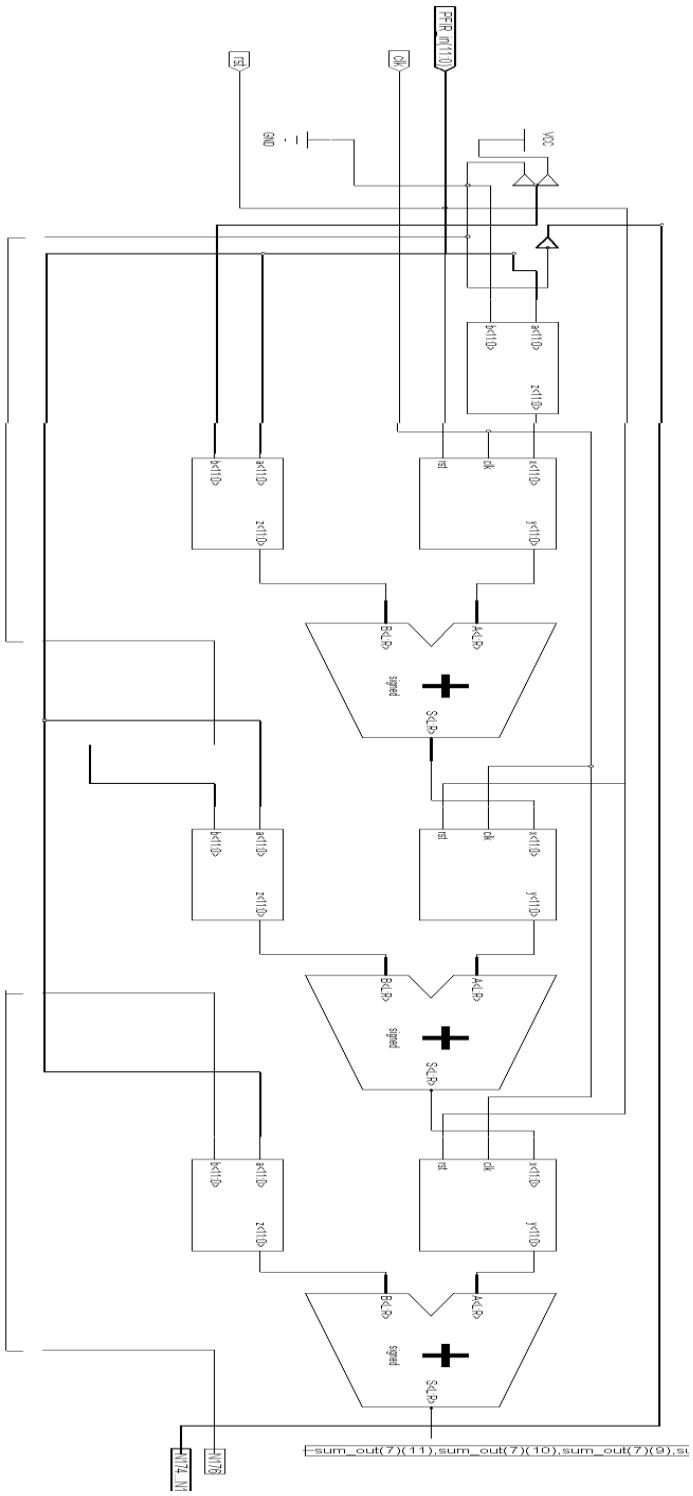


Fig. 6.5 Internal schematic of High Frequency Noise Removal FIR filter

Table 6.2 Pin details of High Frequency Noise Removal FIR filter

Pin	**Direction**	**Detail**
clk(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation we are giving 50 % duty cycle clock signal
rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clock signal
PFIR_in(11:0) (12 bit)	Input	It is 12 bit input to the FIR filter module treated as input of the ECG signal
PFIR_out(11:0) (12 bit)	Output	It is 12 bit output corresponding to FIR filter input PFIR_in module, treated as input of the ECG signal

The Modelsim waveform simulation is shown in fig. 6.6

Step-1: Force reset = '1', then PFIR_output will be zero.

Step 2: Force reset = '0', apply direct clk signal with rising edge. Force PFIR_in = "000000110010" as 12 bit input of the ECG data. The PFIR_out will be PFIR_out = "000000101001".

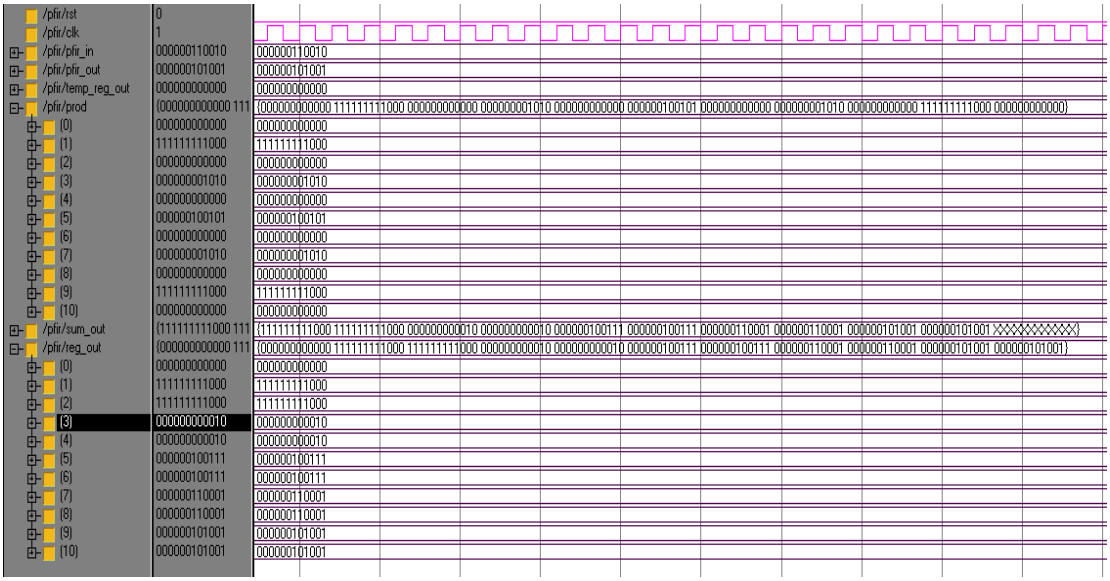


Fig. 6.6 Modelsim Simulation of High Frequency Noise Removal FIR Filter

6.3 Xilinx and Modelsim Simulation of ECG ROM

The RTL view and internal schematic of ECG ROM module is presented in fig. 6.7and fig. 6.8 respectively. The pin details of the ECG ROM chip is given in table 6.3

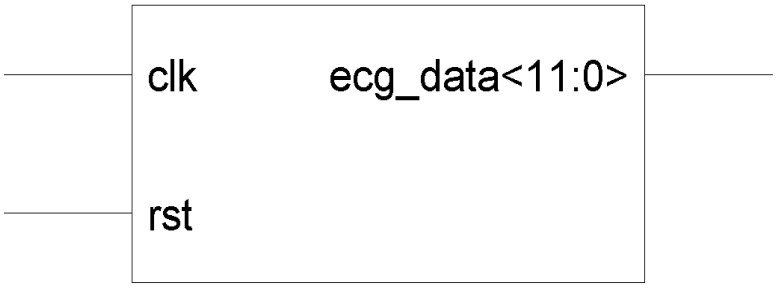


Fig. 6.7 RTL View of ECG ROM module

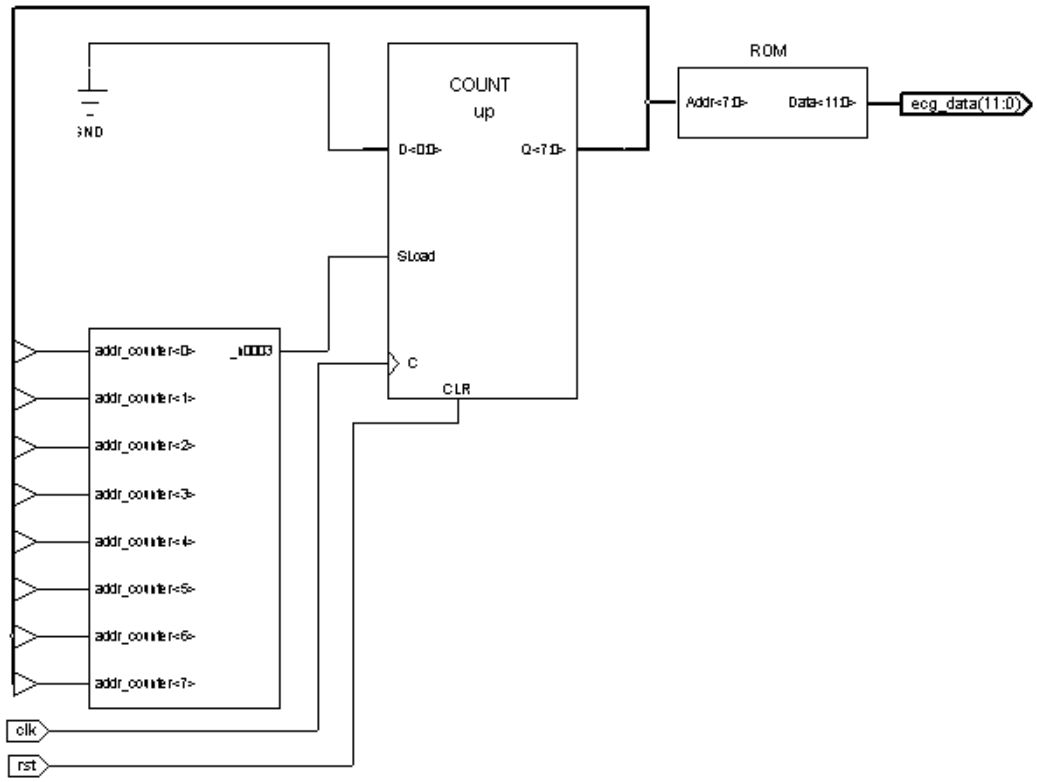


Fig. 6.8 Internal schematic of ECG ROM module

Table 6.3 Pin details of ECG ROM

Pin	Direction	Detail
clk(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation we are giving 50 % duty cycle clock signal
rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clock signal
ECG_data(11:0) (12 bit)	Output	The ECG output data is the 12 bit data when the address counter is 50 then the corresponding ecg signal will be displayed.

The Modelsim simulation waveform is shown in fig. 6.9.

Step-1: Force reset = '1', then ECG_data will be zero.

Step 2: Force reset = '0', apply direct clk signal and ROM address presented by ROM counter ECG_ROM_addr_counter = 50 and ECG_ROM_addr_counter = 51, the corresponding data will be 512 and 462 (decimal) corresponding to the address.

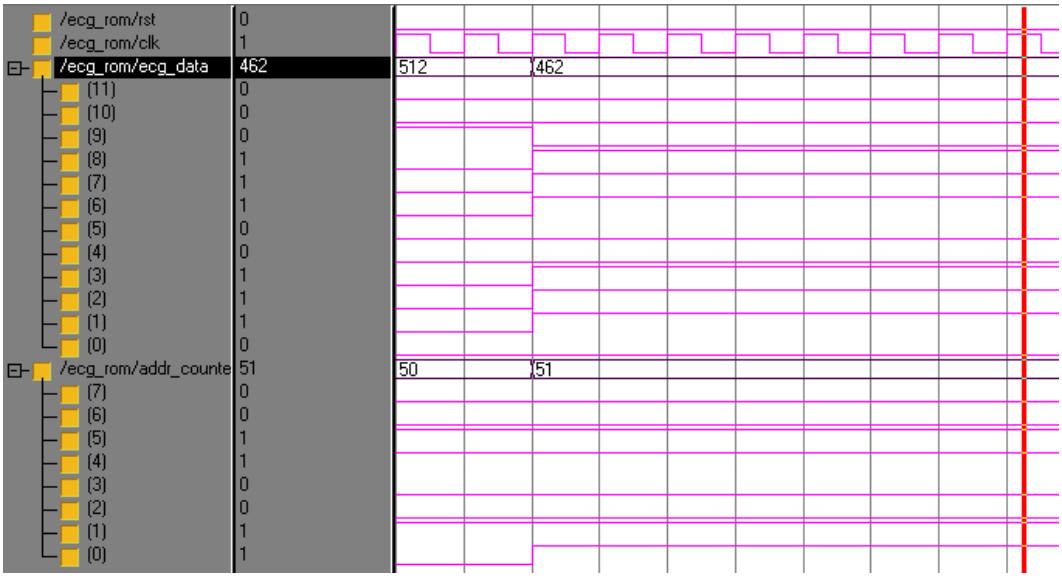


Fig. 6.9 Modelsim Simulation of ECG ROM module

The samples of the ECG signal is generated from MATLAB by using MIT-BIH database and heartbeat is calculated. The same ECG samples are converted into the binary and saved in the ROM of FPGA with the 12- bit data. Rst is the reset used to reset the module or clear previous data. Clk is used for the synchronization. As the clock is given, the values are given to the output, which will result in ECG signal. as addr_counter is a counter which is used as read address generator as address is given to rom block ecg signal is given to output as saved in ROM. The filtered data is stored in the dual port RAM of the FPGA. The 12 bit ECG data is stored in the ROM of the FPGA. In the ECG ROM module the counter counts the values from 0 to 165 after 165 ECG samples it repeats. The array type of 8 which has the possible combination of 2^8=256 but the counter should stop at 165 since the data extracted from MIT-BIH database is of a 2 minutes data. If the address counter is taken as 7-array type then the possible combination may be of 128 ECG samples.

6.4 Xilinx and Modelsim Simulation of ECG Time Domain Analysis Module

The RTL view of the time domain analysis module of ECG signal is shown in fig. 6.10 and corresponding internal schematic in fig. 6.11. The details of the pins is listed in the table 6.4.

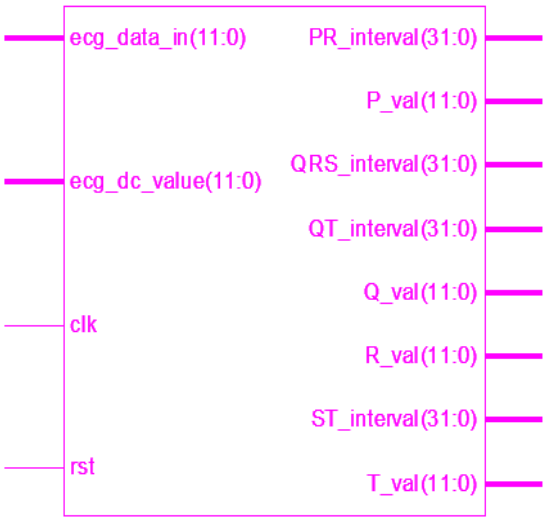


Fig. 6.10 RTL view of ECG Time Domain Analysis Module

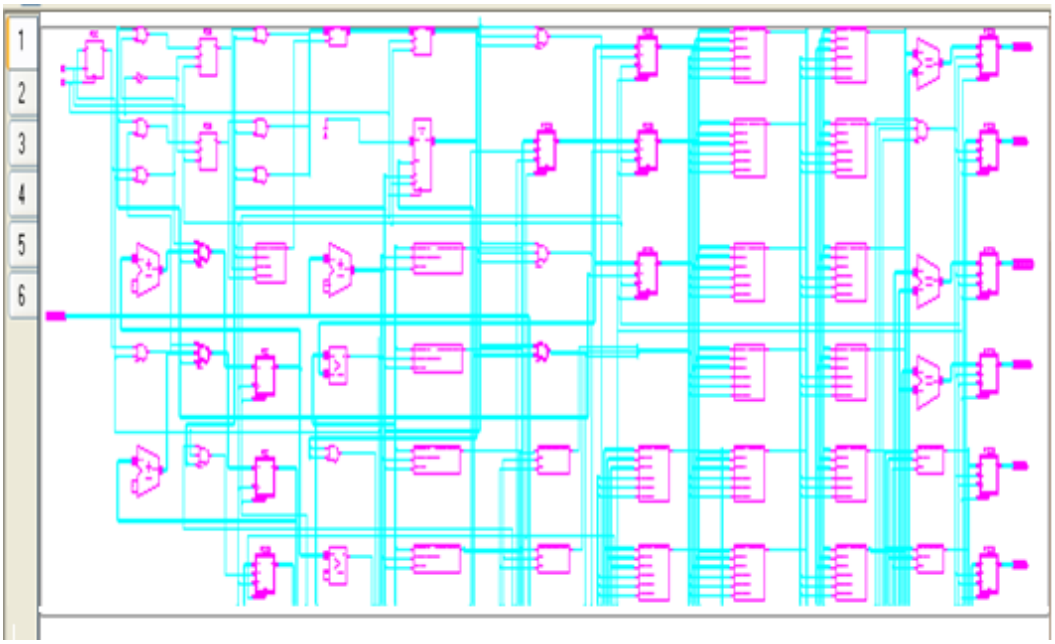


Fig.6.11 Internal schematic of ECG time domain analysis

Table 6.4 Pin details of ECG Time Domain Analysis Module

Pin	**Direction**	**Detail**
clk(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation we are giving 50 % duty cycle clock signal
rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clock signal
ECG_data_in (11:0) (12 bit)	Input	It is the 12 bit data input to preset the incoming of the ECG signal.
ECG_dc_value(11:0) (12 bit)	Input	It is the threshold fixed value (DC value) of as 464 with binary “0001 1101 0000”
P_val(11:0) (12 bit)	Output	Presents the 12 bit output as the magnitude of Q wave
Q_val(11:0) (12 bit)	Output	Presents the 12 bit output as the magnitude of Q wave

R_val(11:0) (12 bit)	Output	Presents the 12 bit output as the magnitude of R wave
T_val(11:0) (12 bit)	Output	Presents the 12 bit output as the magnitude of T wave
PR_interval(31:0) (32 bit)	Output	Presents 32 bit output data as the interval of PR
QRS_interval(31:0) (32 bit)	Output	Presents 32 bit output data as the interval of QRS
QT_interval(31:0) (32 bit)	Output	Presents 32 bit output data as the interval of PR.
ST_interval(31:0) (32 bit)	Output	Presents 32 bit output data as the interval of PR.

The Modelsim simulation waveform is shown in fig. 6.12.

Step-1: Force reset = '1', then present state and next state will be zero.

Step 2: Force reset = '0', apply direct clk signal then the time domain values are extracted as ECG_data_in(11:0) = "512" (decimal) = "001000000000" (binary), ECG_dc_value(11:0) = "464" decimal, = "000111010000" (binary), P_val(11:0) = "685" (decimal) = "001010101101"(binary), Q_val(11:0) = "364" (decimal) = "000101101100", R_val(11:0)= "1024" (decimal) = "010000000000", T_val(11:0) = "603" decimal, = "001001011011" (binary), PR_interval(31:0) = "40" = "00000000000000000000000000101000" (binary), QRS_interval(31:0) = "17" (decimal) = "00000000000000000000000000010001" (binary), QT_interval(31:0) = "63" (decimal) = "00000000000000000000000000111111" (binary), ST_interval(31:0) = 46 (decimal) "00000000000000000000000000101110"(binary). The output of the time domain analysis of one patient-1- P, Q, R, T (12 bit data) is used to represent the exact P, Q, R, T values and time interval PR, QRS complex, QT, ST is the 32 bit data.

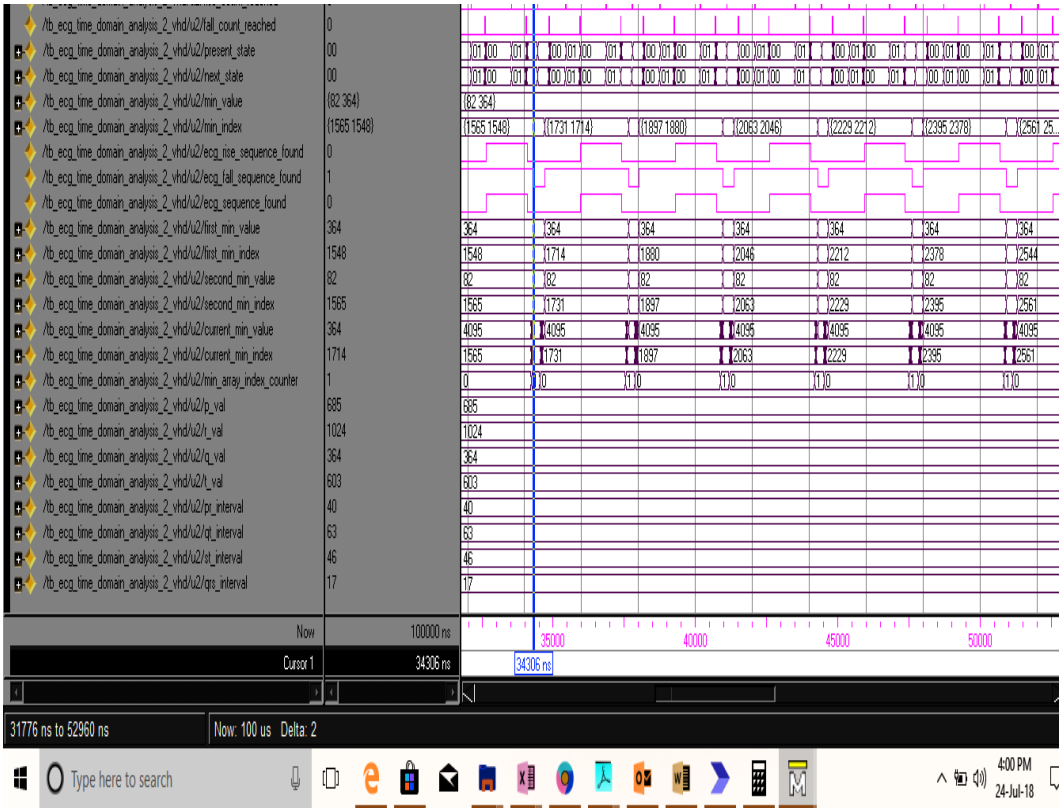


Fig. 6.12 Modelsim simulation of ECG time domain analysis module

The three peaks are found in the max value first corresponds to p then R followed by First max value is p middle max value is R and the minimum values of Q and S. Once the comparison is completed the maximum value and the maximum index is simulated. The maximum value corresponds to the y-axis i.e., voltage and the maximum index corresponds to the X-axis i.e., time. The 2-bit counter is initiated to find the 3 peaks and correspondingly the maximum value and maximum index is noted.

6.5 Xilinx and Modelsim Simulation of Frequency Domain Analysis

The ECG data thus obtained from the ROM is sent for FFT analysis of the ECG signal. The 1024-point FFT [82] is calculated for the ECG signal. The number of channels to observe the output on the chip scope or else in the Digital Storage

Oscilloscope is set as logical high '1'. The hardware target frequency is 50 MHz. The radix-2 decimation in frequency algorithm is used. The output of the FFT is considered as the fixed-point representation with input data being 12 bit X_n real is the 12 bit input data. X_n imaginary value is set to zero since in the input ECG signal has only real values. The output of FFT has real values and imaginary values.23 bits of data correspond to the real values and 23 bits of data corresponds to imaginary values. The unscaled FFT uses 23-bit output data bits and allows adjacent block RAM with less number of multipliers used. The FFT values are stored in the look up table of the device using 3-multiplier structure for the resource optimization technique all the complex multiplications uses the three real multiplications and five add or subtract operations for this structure. The DSP slices are used for the multipliers using the extreme DSP slices and multipliers with 18×18. The optimization techniques reduces the DSP slices and multipliers count, but uses some slice logic. This structure makes use of the DSP slices pre-added to reduce or to remove the need of extra slice logic and hence improves the performance of the system. All the memory data are stored in the block RAM with the resources 4 block RAMs and 6 Multiplier of 18×18.

Table 6.5 FFT output signals

Signals	**Output bits**
X_K REAL	23 bits data
X_K Imaginary	23 bits data
X_n index	10 bits data
X_K index	10 bits data

X_K index is the index of the output data X_n index is the index of the input data. The remaining signals in the RTL are not used. The IP core view of FFT module is given in fig. 6.13 extracted from Xilinx IP Core. The details of the pins is given in table 6.6.

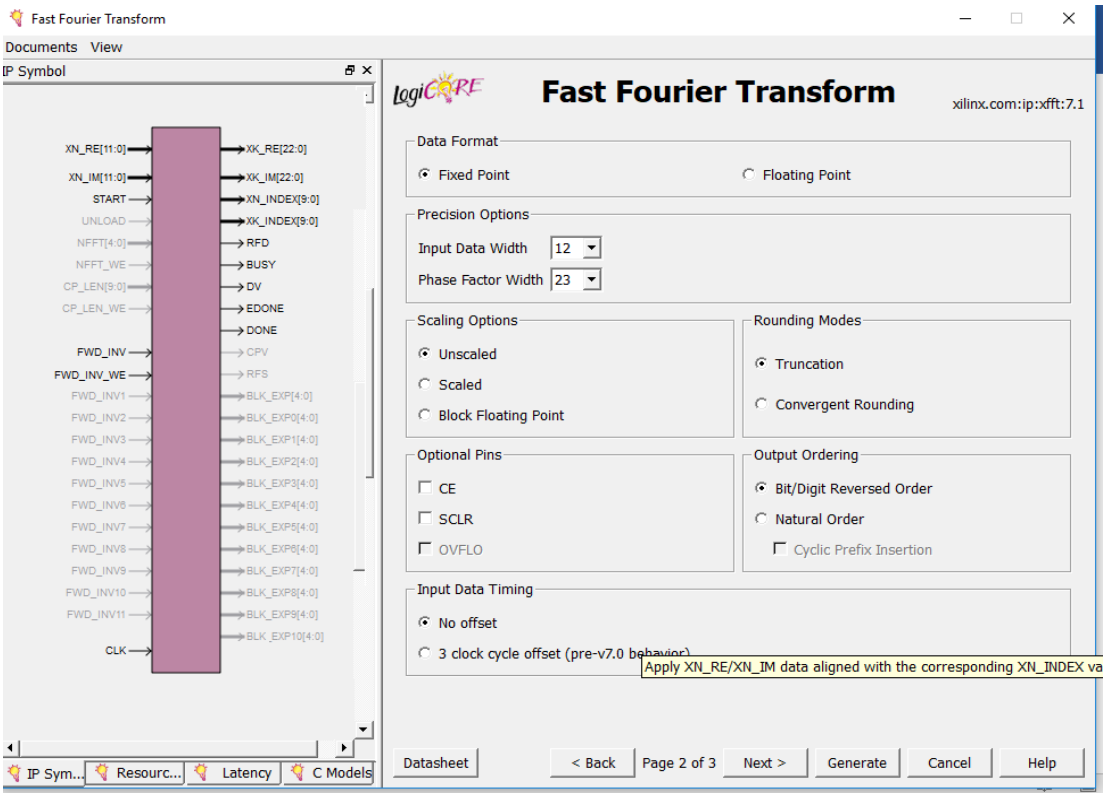


Fig. 6.13 IP core view of FFT

Table 6.6 Pin detail of the FFT core IP

Pin	**Direction**	**Detail**
CLK(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation we are giving 50 % duty cycle clock signal
XN_RE [11:0] (12 bit)	Input	It is the 12-bit ECG signal, presents the real part of input.
XN_IM [11:0] (12 bit)	Input	It presents the imaginary part of 12 bit input ECG signal.
START(1 bit)	Input	Presents the start bit for FFT calculations. It is ‘1’ to assert data bits to begin for loading and transform calculations

FWD_INV(1 bit)	Input	FWD_INV is the 1 bit data. When FWD_INV is '1' then forward transform is calculated. When FWD_INV is '0' then inverse transform is calculated.
FWD_INV_WE (1 bit)	Input	It is active high signal for write enable operation for FWD_INV.
XK_RE [22:0]	Output	It is the 23-bit output data for the real part of the FFT signal.
XK_IM [22:0] (23 bit)	Output	It is the 23-bit output data for the Imaginary part of the FFT signal.
XN_INDEX [9:0] (10 bit)	Input	It is the 10 bit input data index to present $\log_2$ (maximum point size).
XK_INDEX [9:0] (10 bit)	Output	It is the 10 bit output data index to present $\log_2$ (maximum point size).
RFD (1 bit)	Input	It is the control signal for ready for data signal. It is high during load operation.
BUSY (1 bit)	Input	It is treated as core activity indicator, BUSY = '1, 'when the IP core is performing transform.
DV (1 bit)	Input	DV stands for data valid. It is '1' when valid data is presented at the output.
EDONE (1 bit)	Input	It is active high as early done strobe signal. It goes high for one cycle immediately before the Done signal goes high.
DONE (1 bit)	Input	Signal is the FFT complete strobe (Active High). It indicates the status as DONE = '1', when the transitions and transform calculation in one clock cycle is completed.

6.6 Xilinx and Modelsim Simulation of Magnitude Calculation

The FFT has the real and imaginary parts. The approximate equation is used to determine the magnitude for the complex number module implementation in which the real part and imaginary part are combined to produce only the magnitude. The RTL of the magnitude calculation module is presented in fig. 6.14 and its internal schematic in fig. 6.15. The output of magnitude calculation is of 16-bit. The absolute value of real part and imaginary part is considered for the calculation. The sum of real part and imaginary part is taken as approximate equation of magnitude. Table 6.7 presents the pin details of the magnitude calculation module.

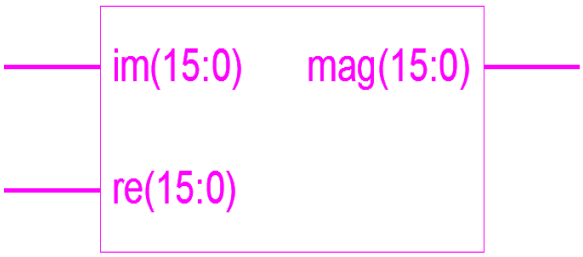


Fig. 6.14 Magnitude calculation module

Table 6.7 Pin details of magnitude calculation module

Pin	**Direction**	**Detail**
Clk(1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation, we are giving 50 % duty cycle clock signal.
rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clk signal
IM(15:0) (16 bit)	Input	It is the 16-bit imaginary input data from the FFT signal.
RE(15:0) (16 bit)	Input	It is the 16 bit real input data from the FFT signal.
Mag(15:0) (16 bit)	Output	It presents the 16-bit output signal to present the exact magnitude of the ECG signal.

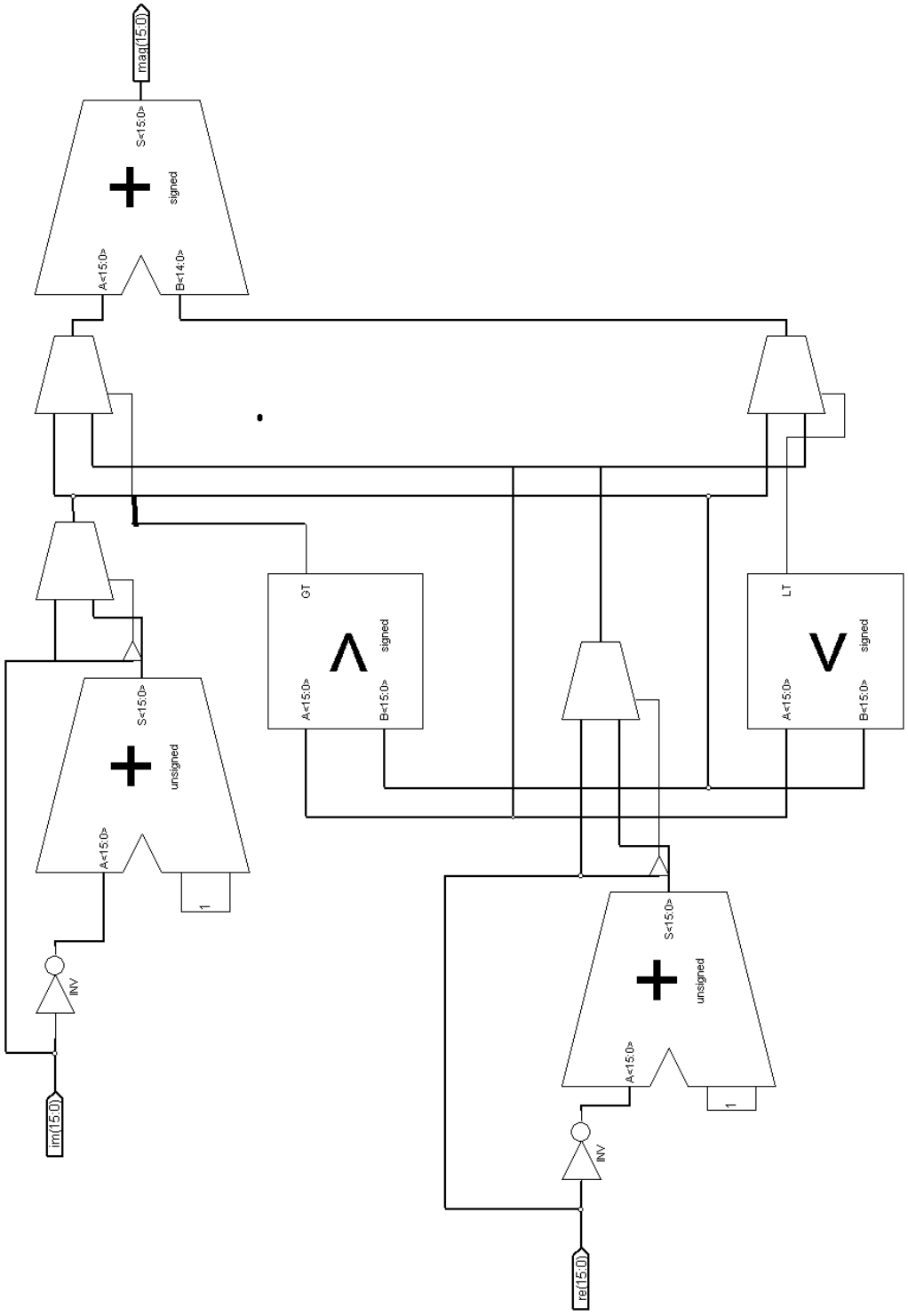


Fig. 6.15 Internal schematic of magnitude calculation module

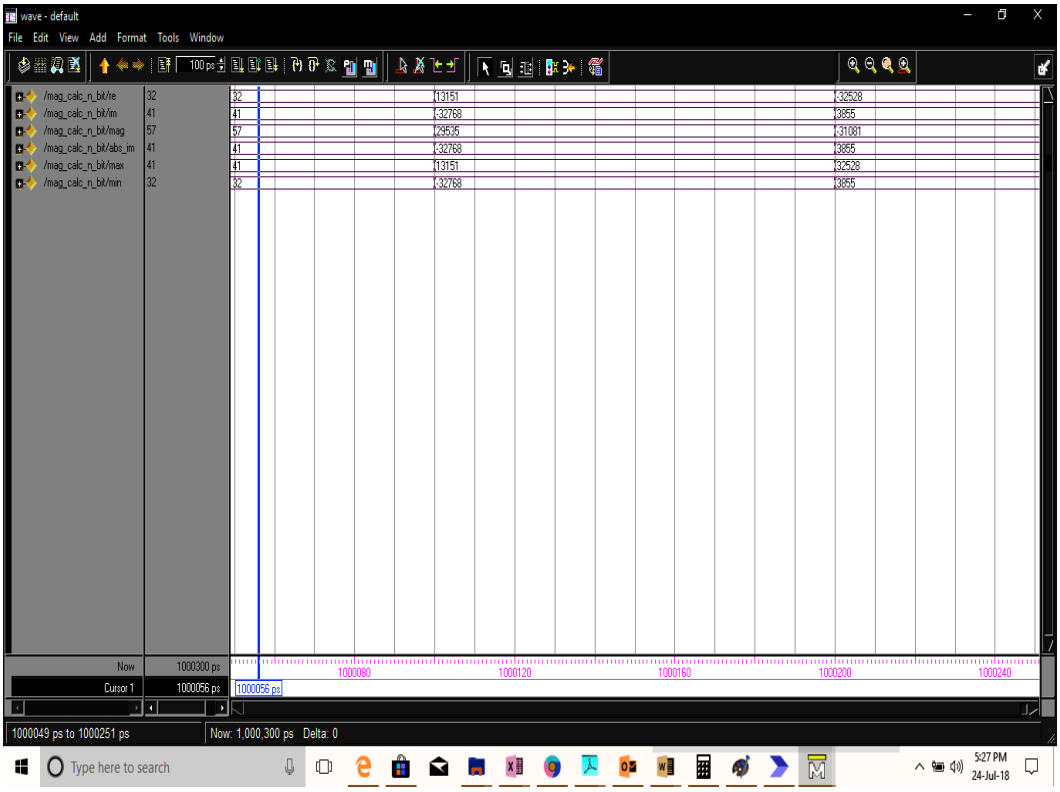


Fig. 6.16 Modelsim simulation waveform for magnitude calculation module

The Modelsim simulation waveform is shown in fig. 6.16.

Step-1: Force reset = '1', then present state and next state will be zero.

Step-2: Force reset = '0', apply direct clk signal. Force IM(15:0) = 41 (decimal) = "0000000000101001", and RE(15:0) = 32 (decimal) = "0000000000100000", then output Mag(15:0) = 57 (decimal) = "0000000000111001" (binary).

This module takes the input from the 1024-point FFT output, which has imaginary and real values as output. First it checks the real and imaginary values are of positive or negative values by checking the signed bit as '1' or '0' if it is '1' then that is assumed as negative value else positive value. Then real values are compared with imaginary values to find maximum and minimum values. Then minimum value is added to maximum value excluding the signed bit of minimum value.

6.7 Xilinx and Modelsim Simulation of Top Level ECG Chip

The RTL view of top level ECG chip and internal schematic is presented in fig. 6.17 and fig. 6.18 respectively. The detail of the pins is listed in table 6.8. The top-down approach is used to structure the top-level chip of ECG module in which all modules are configured and internally port map with different instances and signals.

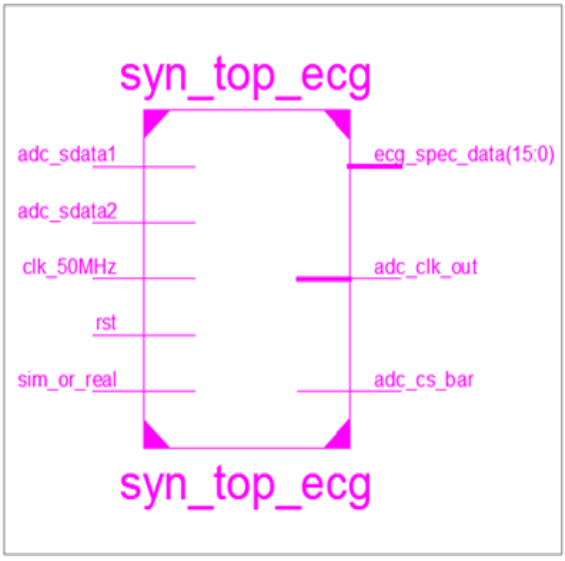


Fig.6.17 RTL view of top level ECG system chip

Table 6.8 Pin detail of top level ECG system chip

Pin	**Direction**	**Detail**
Clk_50MHz (1 bit)	Input	The input used to provide the rising edge of the clock signal. In the simulation, we are giving 50 % duty cycle clock signal.
rst(1 bit)	Input	The input used to keep all the output register contents as zero and synchronized with clk signal.
adc_sdata1(1 bit)	Input	It presents the serial data input 1 of the two port adc input.

adc_sdata2 (1 bit)	Input	It presents the serial data input 2 of the two port adc input.
sim_real (1 bit)	Input	It is the input slight switch and presents the simulation and real input for ECG signal behavior. If switch SW = '0', then the chip work in simulation mode else it works in real time mode.
ecg_spec_data (15:0)	output	It present the 16 bit ECG output corresponding to the ROM memory
adc_clk_out(1 bit)	output	It is the clock out signal for the ADC module ADC S7476MSPS peripheral module (PMOD)
adc_cs_bar (1 bit)	output	It presents the active low input corresponding to the ADC chip select

6.7.1 Modelsim Simulation Results of ECG time domain analysis

The time domain analysis is shown in the below fig. 6.19, in which rst and clk presents the reset and clock signal. The ECG data is of 12 bit input ECG data and ECG_DC_value is the reference value set for the ECG signal because it has 3 rising peaks and two min-max values of P, Q, R, and T wave of 12 bit. The PR, QT, ST and QRS is the time interval of 32-bit data. The Modelsim timing diagram presents the standard values of P, Q, R, T and PR, QT, ST and QRS time interval. ECG_DC_value is set to 464 for the reference threshold value and corresponding the ECG input data is taken and maximum 3 peaks used to find out the max value corresponding to first peak of P then R is following first max value is p middle max value is R and the minimum values of Q and S. Once the comparison is completed the maximum value and the maximum index is simulated. The maximum value corresponds to the y-axis i.e., voltage and the maximum index corresponds to the X-axis i.e., time-period. The 2-bit counter is initiated to find the three peaks and correspondingly the maximum value and maximum index is noted.

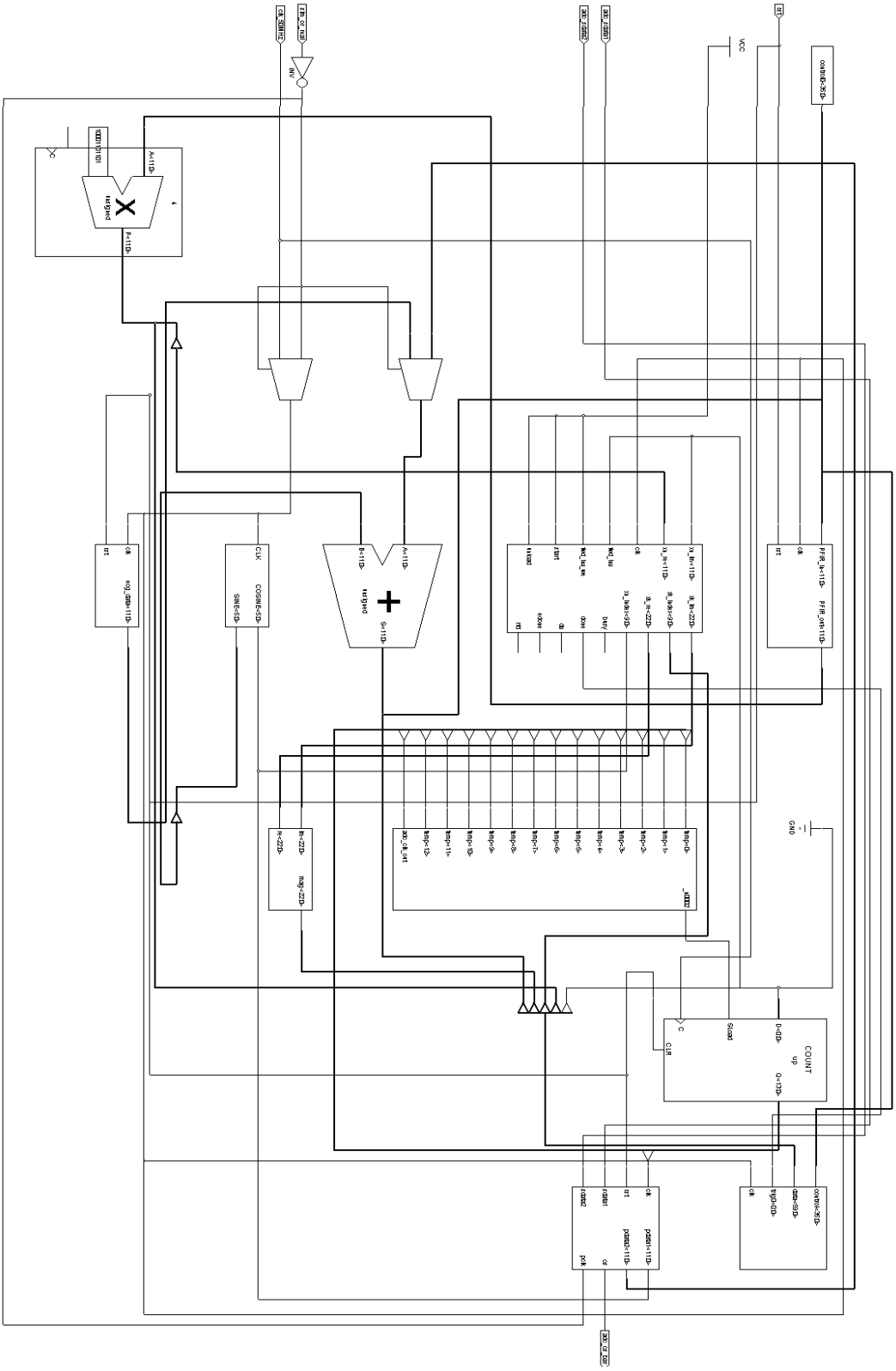


Fig. 6.18 Internal schematic of top level ECG chip

The simulation diagram in fig.6.19 has max value (685, 1024, 603) in order to represent ‘P’ value 685 as 12 bit binary data. The same 12-bit binary representation is used to represent ‘R’ i.e., 1024 and similarly 603 for ‘T’. The index (X-axis) is represented with 32 bits (4837, 4877, and 4931). ECG_data_1 is input that can be from rom block or external input applied by MATLAB (practical ECG input applied by ADC). DC_value is the zero origin of ECG signal because ADC is an unsigned so cannot predict negative values. The positive and negative peaks are calculated by taking DC_value as reference, max_value and max_index are the peak values of P, R, T and min_value and min_index for Q and T, which are generated by simulated ECG results.

Fig. 6.19 ECG time domain analysis

The Modelsim simulation results of ECG signal with noise removal signal is presented in fig. 6.20.

Fig. 6.20 ECG signal and noise removal signal

In simulation waveform reset and clock are the inputs clock with the 50 MHz is the system clock. The simulation or real is a one-bit data. When the sim_or_real is '0' then the deals of the patient is recorded in the simulation model [77] and when sim_or_real is "1" the input is given from the patient by physically connecting the ECG heart beat sensors. The two-port channel ADC is used where ADC_Sdata1 is the one channel serial data, adc_sdata2 is the second channel serial data adc_clk_out, and adc_cs_bar are the outputs of the ADC S7476MSPS peripheral module (PMOD) connector.

ECG_DC_Value is the 12-bit DC value for reference input.ECG_Data_in is the input ECG data from the ROM memory of the FPGA. ECG_data_with_noise is the ECG signal with the noise added to the noise is the direct digital synthesizer (DDS) IP core from the XILINX[80] the 6 bit sine wave is added. The noise removal filter FIR filter with direct form II is used to remove the noise. The filter coefficients are generated by using the MATLAB and these filter coefficients are given as an input to the ECG signal with noise and the output of the noisy ECG signal is the ecg_data_with_noise_filterd. ECG_data_with_noise is the 12-bit data and the ECG_data_with_noise_filterd is the 12-bit data. The time domain analysis is carried out after the noise removal signal and the time domain parameters of patient 1 is carried out and the simulation waveform of fig.6.21 is shown. The details of the time domain parameters are shown in table no 6.9

Table 6.9 Time domain values of ECG signal

Amplitude(mv)	**Duration(time interval) in seconds**
P wave 662	P-R interval 20
R wave 1023	Q-T interval 43
Q wave 329	S-T interval 46
T wave 580	QRS interval 17

The patient -1 details are compared with the standard ECG data [64] and table 1. The DC reference value is 384 and let it be M.

'P' value is 662 - 464 = 198

'R' value is 1023 - 464 = 559

'Q' value is 329 – 464 = -135

'T' value is 580 – 464 = 116

Fig.6.21 ECG signal with P, Q, R, S and T values

6.7.2 Modelsim Simulation of 1024 -point FFT

The simulation waveform of FFT is shown in fig. 6.22 with parameters Fwd_inv_we is a one-bit data, which indicates if a forward FFT transform or an inverse FFT transform is performed. When FWD_INV_WE = '1' a forward transform is connected. If FWD_INV_WE =0, an inverse transform is computed. It goes low during the loading of data into the FFT. Data is only transferred when FWD_INV_WE goes High. It can assert a significant time before sample processing actually begins. It goes low during the unloading of data from the FFT. Data is still only transferred when High. FFT start signal is active high when START is asserted to begin the data loading and transform calculation. For streaming I/O, START begins data loading, which proceeds directly to transform calculation and then data unloading. DV stands for Data valid (Active High) when

the signal is high when valid data is presented at the output. SCALE_SCH_WE is the Write enable for SCALE_SCH (Active High) This port is available only with scaled arithmetic since ‘x’ is used. DONE signal is the FFT complete strobe (Active High) DONE transitions High for one clock cycle when the transform calculation has completed. Busy signal is Core activity indicator (Active High) this signal goes high while the core is computing the transform. Edone is the signal early done strobe (Active High). Edone goes high one clock cycle immediately prior to done going High. XN_RE is the input data bus of 12 bit Real component in two’s complement or single precision floating-point format. XK_IM is the output data bus of 23 bits. XK_INDEX is the Index of output data.

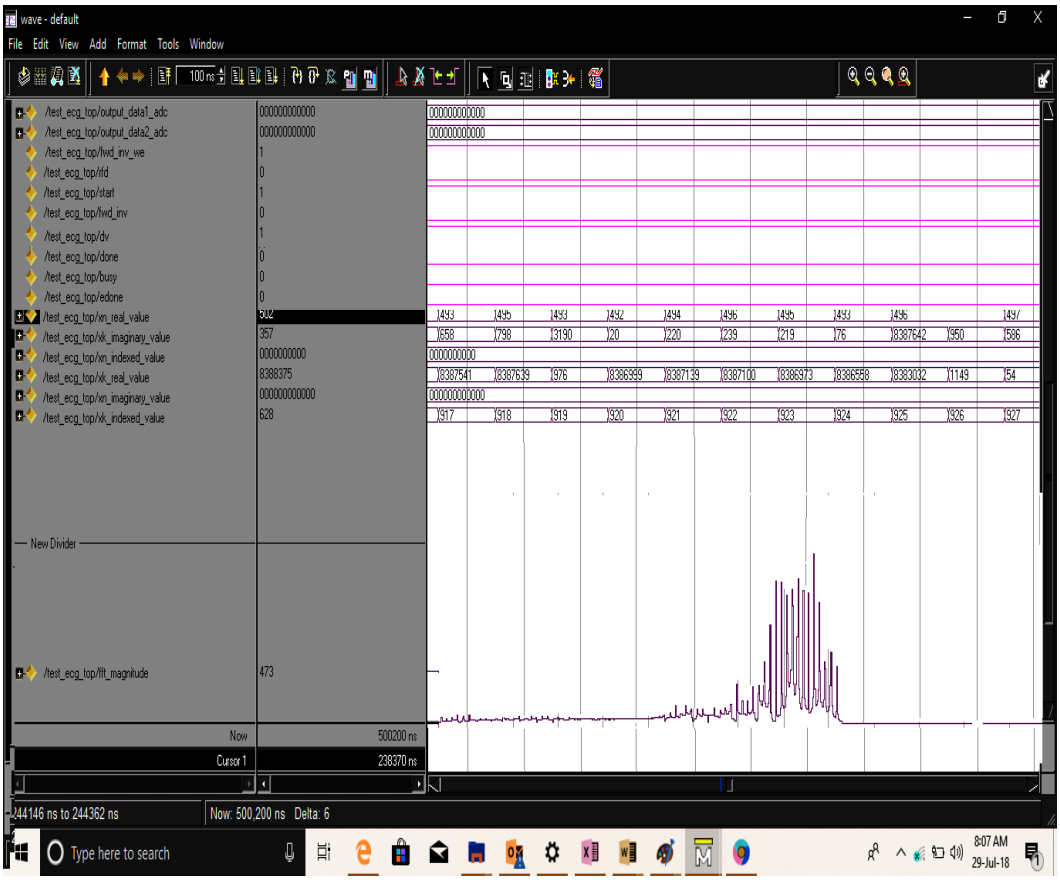


Fig. 6.22 ECG signal with FFT parameters.

The Fast Fourier transform of the 1024 point is calculated and the xk index 1023, which shows the time, index as shown in below fig. 6.23. As filtered ECG signal is

given to the FFT, the FFT output is real and imaginary part. To plot the FFT output the signals needed to add real and imaginary part so mag signal is combined output of the real and imaginary part of the signals.

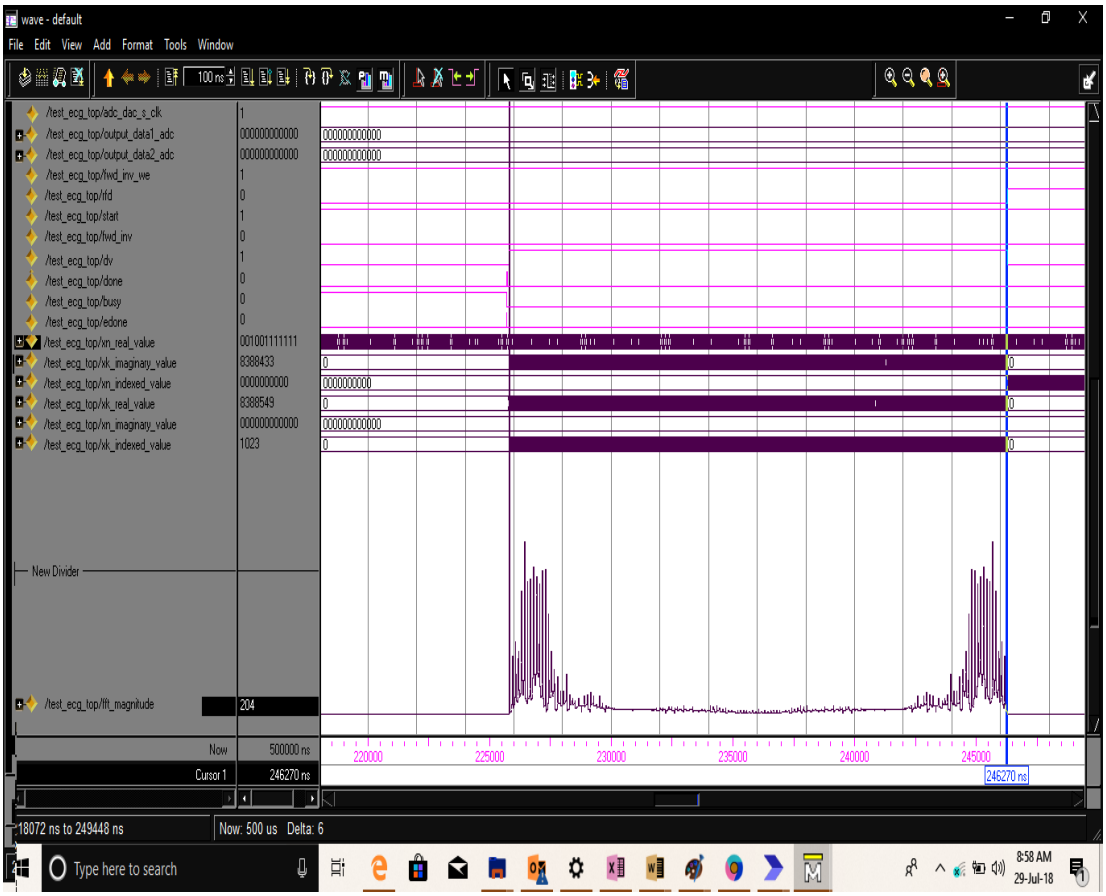


Fig.6.23 FFT (1024 point) and its magnitude

The DDS core is the inbuilt feature in the Xilinx. It help the designer to design large-scale architecture. To design 1024 point FFT, the 64-point FFT is directly configured from DDS core. The pipelined architecture and parallel processing makes the system fast and reliable for the scaled architecture of 1024 point FFT based on ping-pong design scheme listed in fig 6.24. The 16 blocks are used to represent the 1024-point FFT with the help of 64 point FFT. In the same way 8, 4, 2 blocks are used to present 128 point, 256 point, 512 point FFT. The 16 FFT modules are considered with Time scale T1… T16. The architectures support the

parallel and concurrent execution of the FFT modules. The Modelsim waveform of the 64-point DDC core FFT module is shown in fig. 6.25.

<table>
<tr><td>T1</td><td>FFT-64</td><td>FFT-128</td><td rowspan="4">FFT-256</td><td rowspan="8">FFT-512</td><td rowspan="16">FFT-1024</td></tr>
<tr><td>T2</td><td>FFT-64</td><td rowspan="3">FFT-128</td></tr>
<tr><td>T3</td><td>FFT-64</td></tr>
<tr><td>T4</td><td>FFT-64</td></tr>
<tr><td>T5</td><td>FFT-64</td><td rowspan="3">FFT-128</td><td rowspan="4">FFT-256</td></tr>
<tr><td>T6</td><td>FFT-64</td></tr>
<tr><td>T7</td><td>FFT-64</td><td rowspan="2">FFT-128</td></tr>
<tr><td>T8</td><td>FFT-64</td></tr>
<tr><td>T9</td><td>FFT-64</td><td rowspan="3">FFT-128</td><td rowspan="4">FFT-256</td><td rowspan="8">FFT-512</td></tr>
<tr><td>T10</td><td>FFT-64</td></tr>
<tr><td>T11</td><td>FFT-64</td><td rowspan="2">FFT-128</td></tr>
<tr><td>T12</td><td>FFT-64</td></tr>
<tr><td>T13</td><td>FFT-64</td><td rowspan="3">FFT-128</td><td rowspan="4">FFT-256</td></tr>
<tr><td>T14</td><td>FFT-64</td></tr>
<tr><td>T15</td><td>FFT-64</td><td rowspan="2">FFT-128</td></tr>
<tr><td>T16</td><td>FFT-64</td></tr>
</table>

Fig. 6.24. FFT-1024 Realization using FFT-64 as DDS core

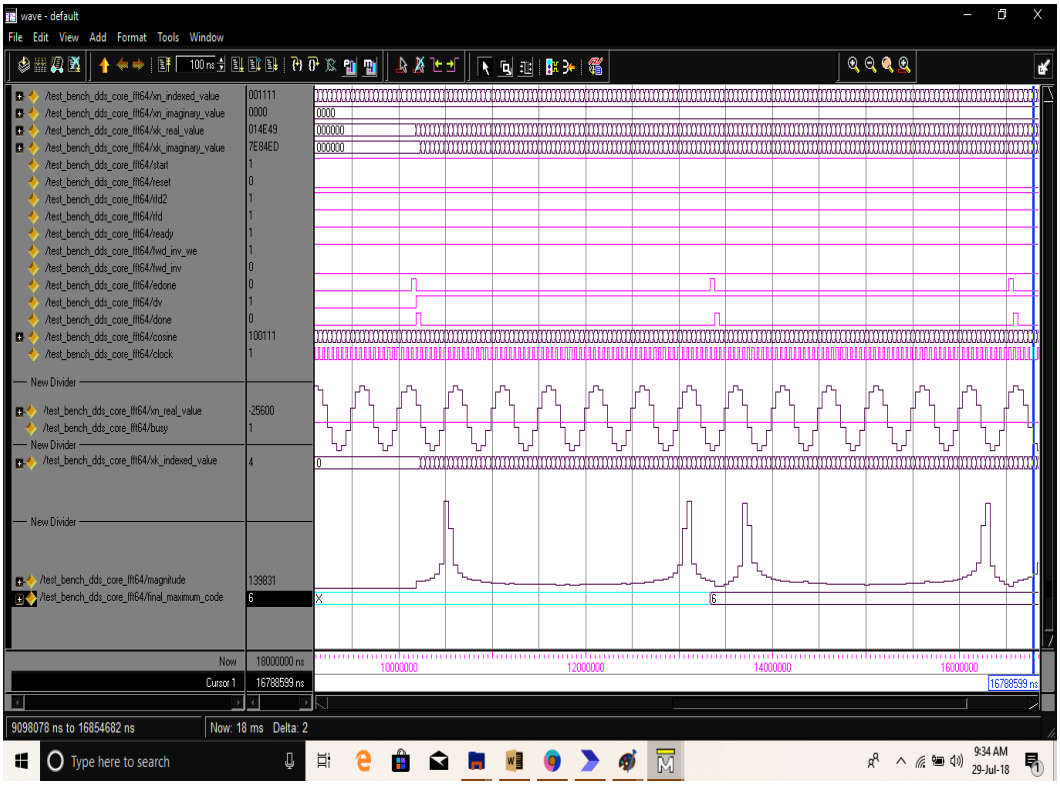


Fig. 6.25 FFT (64 point) and its magnitude

In the simulation of 64-point FFT first peak is at index 6 and the next peak is at index 58. In the same way, the next peaks are observed at index 6, till the computation of 1024 points. The sine and cosine values are stored on the ROM memory. The observed values help to test the functionality of FFT to analyze the signal from time to frequency domain.

CHAPTER 7

FPGA SYNTHESIS AND VERIFICATION

The chapter details the Virtex 5 FPGA synthesis environment, FPGA synthesis process, experiment setup and chip scope analyzer for real time signal processing in FPGA. The chapter also discusses the QRS detection and R peak detection from the synthesized test cases, comparative analysis with respect to hardware and timing utilization report extracted from FPGA devices. It also compares with the works done by different existing researchers and estimating the comparative system errors on data extracted from 30 patients of MIT-BIH.

7.1 FPGA Synthesis

The synthesis process is carried out on Xilinx Virtex – 5 XC5VLX110T Digilent manufactured FPGA as shown in fig. 7.1. It has two Xilinx XCF32P [41, 42] platform flash ROMs for storing large device configurations of 32 MByte each, 64 bits wide 256 Mbythete DDR2 modules compatible with Embedded Development Kit (EDK) supported IP and software drivers. It has in board 32-bit synchronous Zero Bus Turnaround (ZBT) SRAM and Intel P30 Strata Flash. It supports 10/100/1000 tri-speed Ethernet PHY supporting Media Independent Interface (MII), Gigabit Media Independent Interface(GMII), Reduced Gigabit Media Independent Interface (RGMII), and Serial Gigabit Media Independent Interface (SGMII), Universal Serial Bus (USB) host and peripheral controllers, programmable system clock generator [47, 48]. It has Stereo Audio Codec (SAC) 97 with line in, line out, headphone, microphone, and Sony/Philips Digital Interface Format (SPDIF) digital audio jacks, RS-232 port, 16 x 2 character LCD, I/O devices and ports [43].

Fig. 7.1 Pictorial view of FPGA Virex -5 FPGA [48]

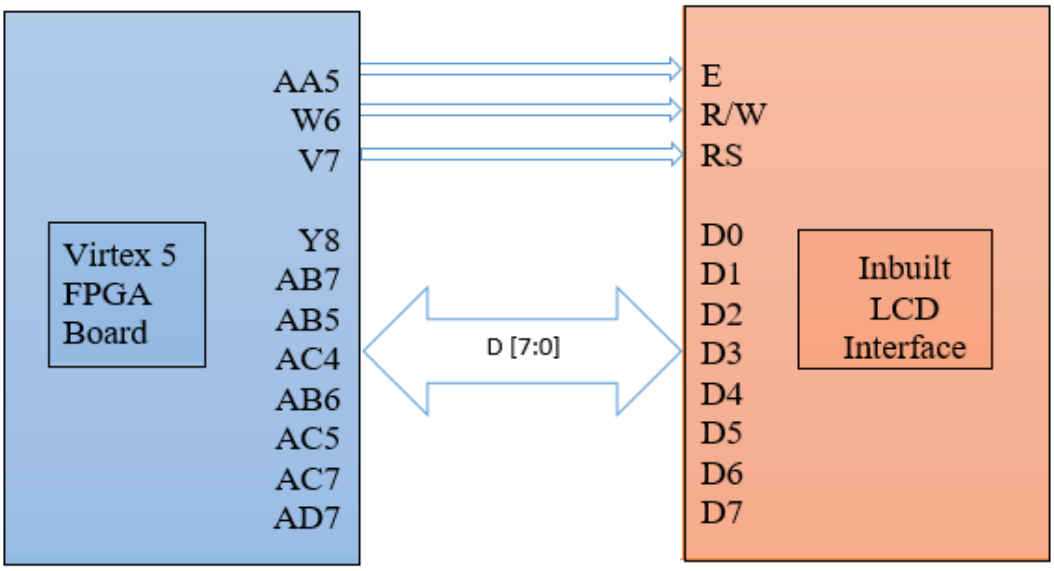


Fig. 7.2 LCD Interface of FPGA [44, 48]

In the synthesis process the programmed in burned in the ROM memory of FPGA. The Virtex-5 FPGA has inbuilt LCD controller, contains character-generator ROM (CGROM) with 208 fixed 5 × 8 character patterns, a character-generator RAM (CGRAM) used to hold eight user-defined 5 × 8 characters, and

one display data RAM(DDRAM) memory which can hold 80 character codes. The character codes are written into the DDRAM memory, which serves as the indexes into the CGROM (or CGRAM). The character code is written into the specific DDRAM memory location and it causes the related characters to appear at the consistent display location. The display locations are shifted right side or left side by setting one bit in the instruction register (IR). The IR register directs the LCD operations and direct display operations such as shift left or right, clear display, set DDRAM address. Fig.7.2 shows the interface diagram of the LCD (16 x 2) to Virtex 5 FPGA. The LCD unit is 16-pin connector in which pins 15 and 16 are not used and applicable for optional backlight. The remaining 14-pin interface has three control signals, eight data signals, and three voltage supply signals. The eight-bidirectional data bus signals interconnect data to the control registers or RAM locations. The RS (Register Strobe) signal clocks data into registers or into RAM, the R/W signal determines bus direction, and the E signal enables the bus for read or write operations. The user constraint file (UCF) is used to lock the FPGA pins. The details of the pins is given in table 7.1.

Table 7.1 UCF pin details in FPGA synthesis

Input Logic	**Pins**	**Description**
clk	N15	Input clock pulse
RS	V7	It is the register select input, high for data, low for instructions.
R/W	W6	Read/write control signal: R/W= 1 for read, and R/W = 0 for write
E	AA5	Read/write enable input high for OE, falling edge writes data
DB0	Y8	Input data bit of bidirectional data bus 0
DB1	AB7	Input data bit of bidirectional data bus 1
DB2	AB5	Input data bit of bidirectional data bus 2
DB3	AC4	Input data bit of bidirectional data bus 3

DB4	AB6	Input data bit of bidirectional data bus 4
DB5	AC5	Input data bit of bidirectional data bus 5
DB6	AC7	Input data bit of bidirectional data bus 6
DB7	AD7	Input data bit of bidirectional data bus 7
Vss	Unassigned	It is the ground input
Vdd	Unassigned	5V input for power supply
Vo	Unassigned	Contrast voltage input (typically 100mV-200mV) at 20^0 C

7.2 Experimental Set-Up

The experiment is carried out to validate the ECG signal processing in real time on Virtex -5 FPGA. Two 9-pin RS-232 [47] ports assist in the transmission of serial data to and from the FPGA board. 100 MHz clock oscillator is the system clock provides the clock signal to the various events taking place within the FPGA and the various programs that require clock for their working. A Digital clock manager is used to reduce the frequency of the system clock. This feature is useful for the task which needs smaller clock frequency [42]. On board USB based FPGA [41, 47] download and debug interface is also present in the Virtex-5 kit where the programmable file is dumped into the FPGA via the USB based download cable. This feature is beneficial in the testing of the programs. There are 8 LEDs on the board, which glow based on the logic 'High' and logic 'Low' of output data, to justify the correctness of data transfer. Hence the LEDs can be interfaced to show the output of a single bit. Four slide switches and four push button switches are used to give the inputs to the FPGA board. They can also act as the reset switches for the various programs. The Kit also has four outputs, SPI based on board Digital to Analog Converter (DAC), which is interfaced to give the analog output to the digital data values. Two inputs, SPI based [42, 48] Analog to Digital Converter (ADC) with programmable gain preamplifier converts the real world analog signals into digital values.

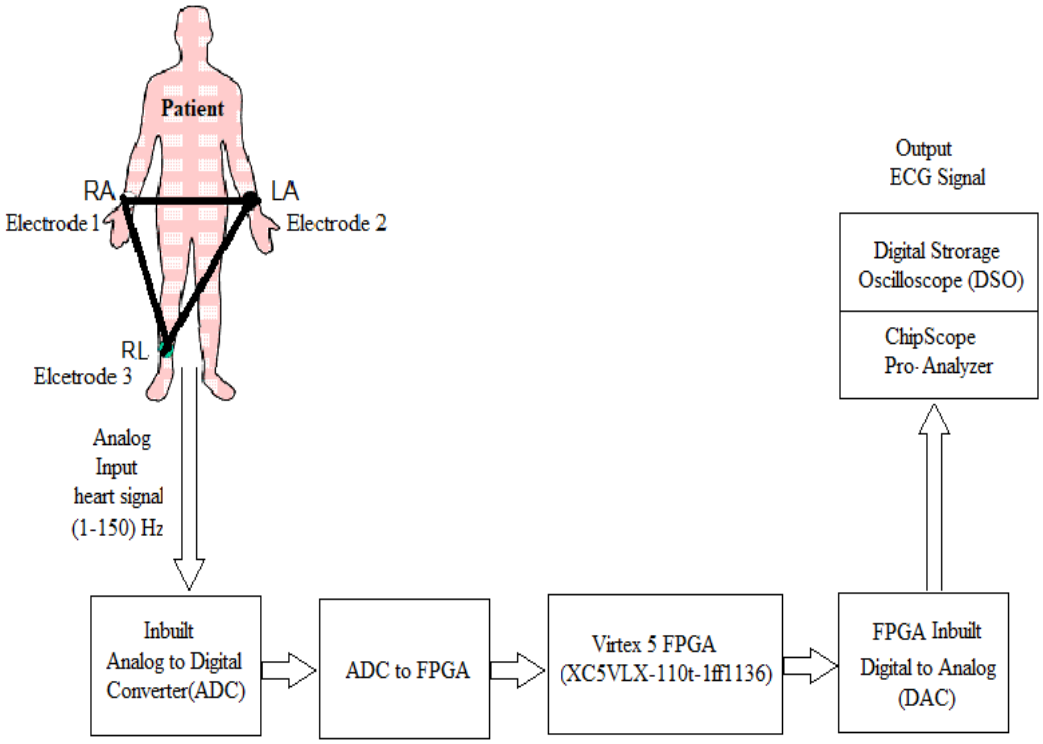


Fig. 7.3 Block diagram of experimental set up

The complete experimental setup and functional flow is shown in fig. 7.3. The three electrodes, electrode-1(RA), electrode-2(LA), and electrode-3 (RL), are placed on the patient's body. The generated analog heart signal is given to inbuilt analog to digital converter (ADC) of FPGA to convert the analog signal (1-150 Hz) to digital as FPGA process the digital signal. The ADC processed signal passes through the Virtex 5, XC5VX-110t-1ff1136 device with the burned synthesized program through Xilinx simulator. Then the signal is converted to digital domain with the help of inbuilt digital to analog (DAC) and ECG signal is shown on Digital Storage Oscilloscope(DSO). It guarantees the successful processing of the ECG signal through FPGA. The experimental set up and generated signal on DSO is shown in fig. 7.4 and fig. 7.5 respectively. The real time heart beat of patient is also verified through FPGA and LCD module depicts the patient real status. The verification is also shown in fig. 7.6 (a) and (b) respectively.

Fig. 7.4 ECG real time ECG signal processing set-up

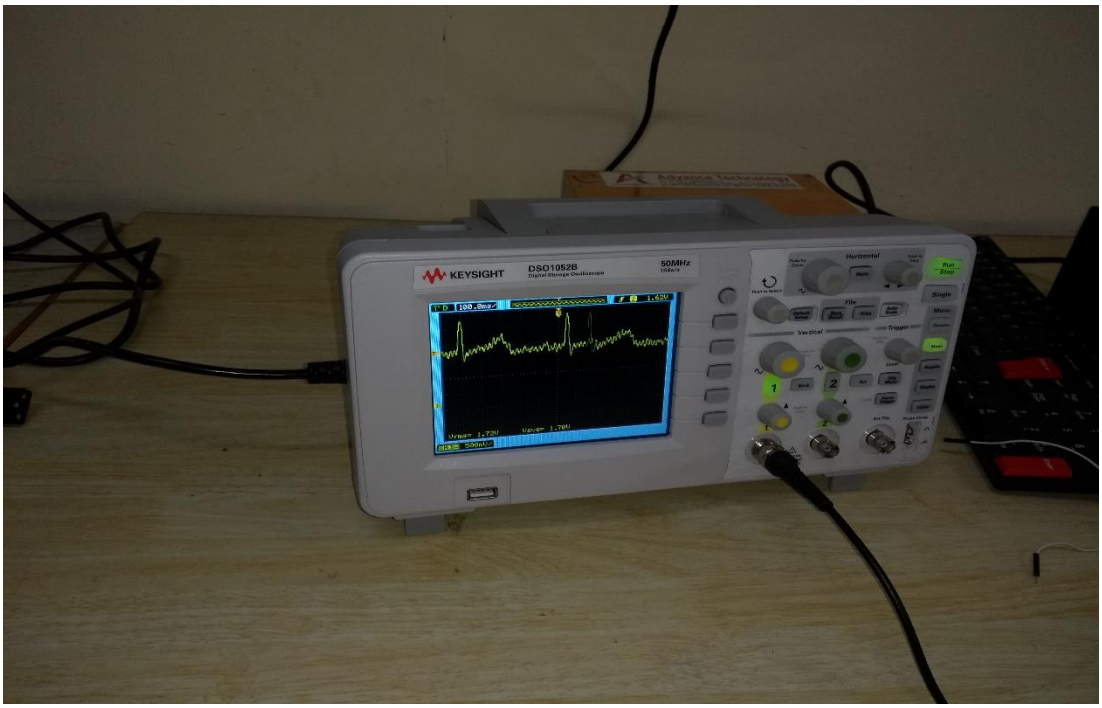
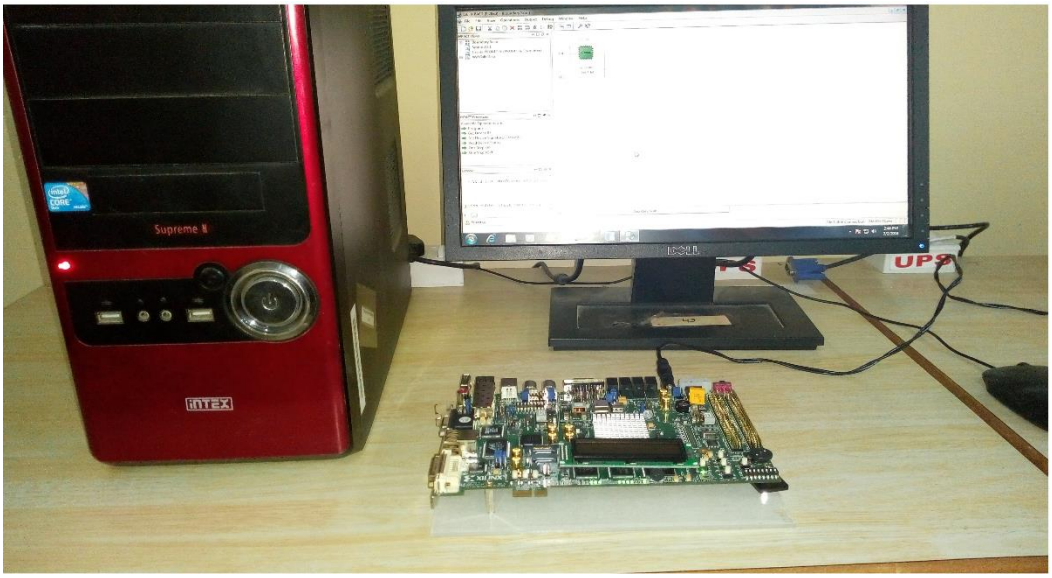
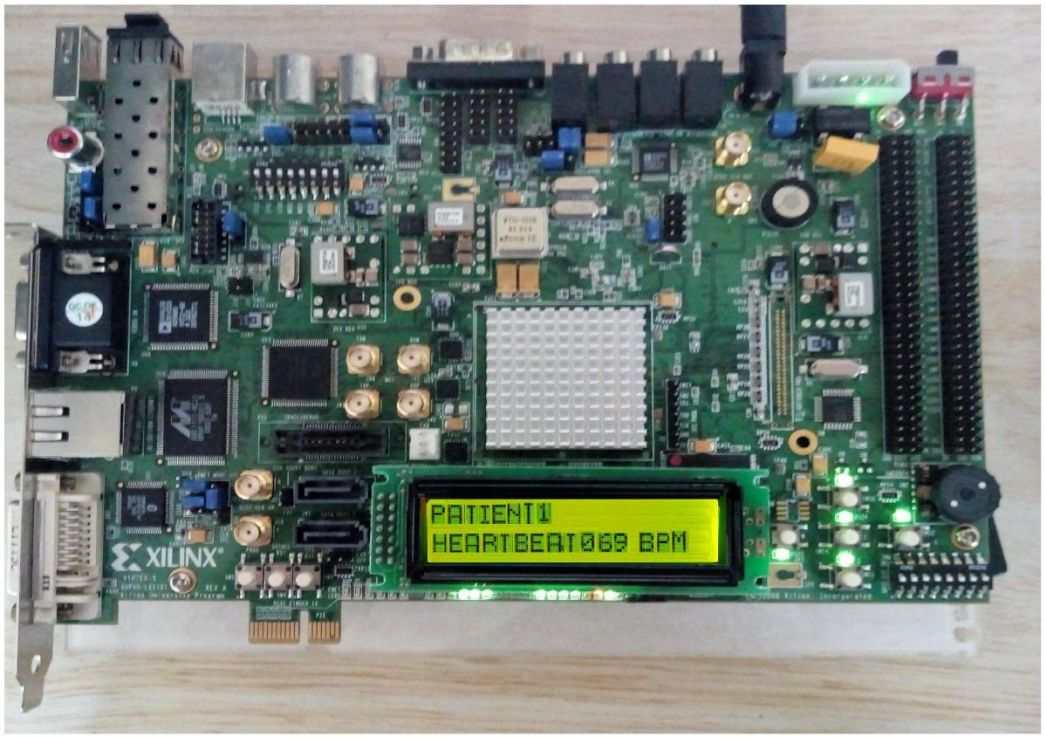


Fig. 7.5 Corresponding signal on DSO



(a) FPGA Connection to PC



(b) Patinet -1 heart beat display

Fig. 7.6 Experimental verification on LCD

7.3 FPGA Signal Analysis on Chip Scope Pro-Analyzer

The ECG signal is also analyzed on Xilinx Chip Scope Pro-Analyzer [40]to check whether the signal is processing in FPGA in real time or not. The signal can be understood with the help of QRS detection algorithm.

7.3.1 QRS Complex Signal Detection

The block diagram for the QRS complex detection [72, 81] process is shown in fig. 7.7. The ECG signal is the input from the physionet [38] database the preprocessing stage is the low pass filter and the high pass filter. These filters are used to remove the power line frequency noise the second low pass filter that is used with the cut-off frequency.

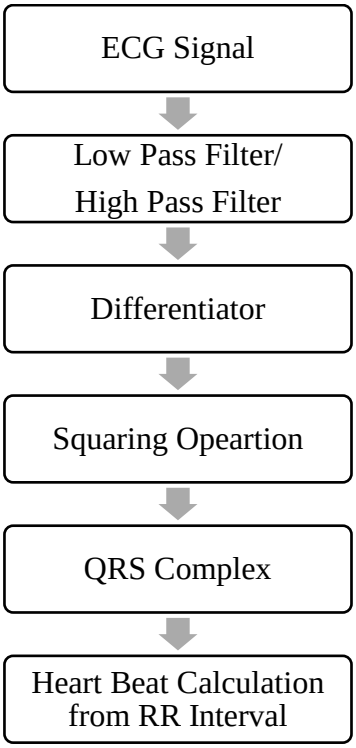


Fig. 7.7 Block diagram to detect R peak from QRS Complex, ECG signal

Low Pass Flter: The second order low pass filter has a transfer function

$$H(Z) = \frac{(1 - Z^{-6})^2}{(1 - Z^{-1})^2} \tag{7.1}$$

The corresponding difference equation is

$$Y(\mathrm{nT}) = 2y(\mathrm{nT}-\mathrm{T}) + x(\mathrm{nT}) - 2x(nT-6T) + x(nT-12T) \quad (7.2)$$

Where 'T' is the sampling period and 'n' is the arbitrary integer. The cut-off frequency of the filter is about 11 Hz from the FFT analysis and implemented with the direct form-II structure.

High Pass Filter: The high pass filter comes after the low pass filtering stage to remove the low frequency or DC offset signal and set it to a zero level. This HPF has a cut-off frequency of 5Hz.The difference equation for the HPF is given by

$$y(nT) = y(nT-T) + \frac{x(nT)}{32} + x(nT-16T) - x(nT-17T) + \frac{x(nT-32T)}{32} \quad (7.3)$$

Implemented with the direct form-II structure. The two filters act as a band pass filter for 5 to 10 Hz and eliminates the DC component and the high frequency noise.

Differentiation Filter: The derivative filter is used to find the slope information of the ECG signal. This technique of finding the slope is the popular among all the ECG analysis algorithm. The reason is that QRS algorithm tends to have larger variation in its slope than all the other features in the waveform of difference equation and the transfer function of the filter is given below.

$$Y(nT) = \frac{2x(nT) + x(nT-1) - x(nT-3) - 2x(nT-4)}{8} \quad (7.4)$$

$$H(Z) = \frac{2 + Z^{-1} + Z^{-3} - 2Z^{-4}}{8} \quad (7.5)$$

The fig. 7.8 is the simulated and synthesis real-time chipscope waveform peaks for ECG QRS complex, can be used to calculate heartbeat based on the R-R interval [85, 97, 99]. The output is showing on the chipscope pro analyzer software. X- axis represents the time in seconds and Y-axis represents the amplitude of the signal.

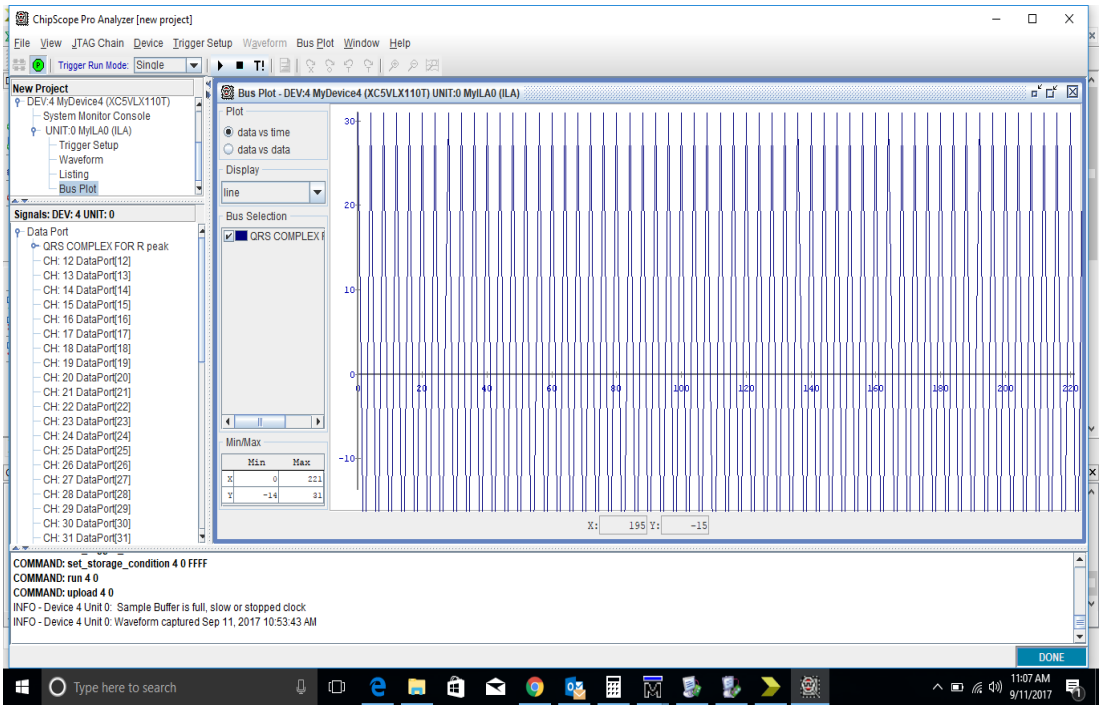


Fig.7.8 QRS complex wave peaks in chipscope.

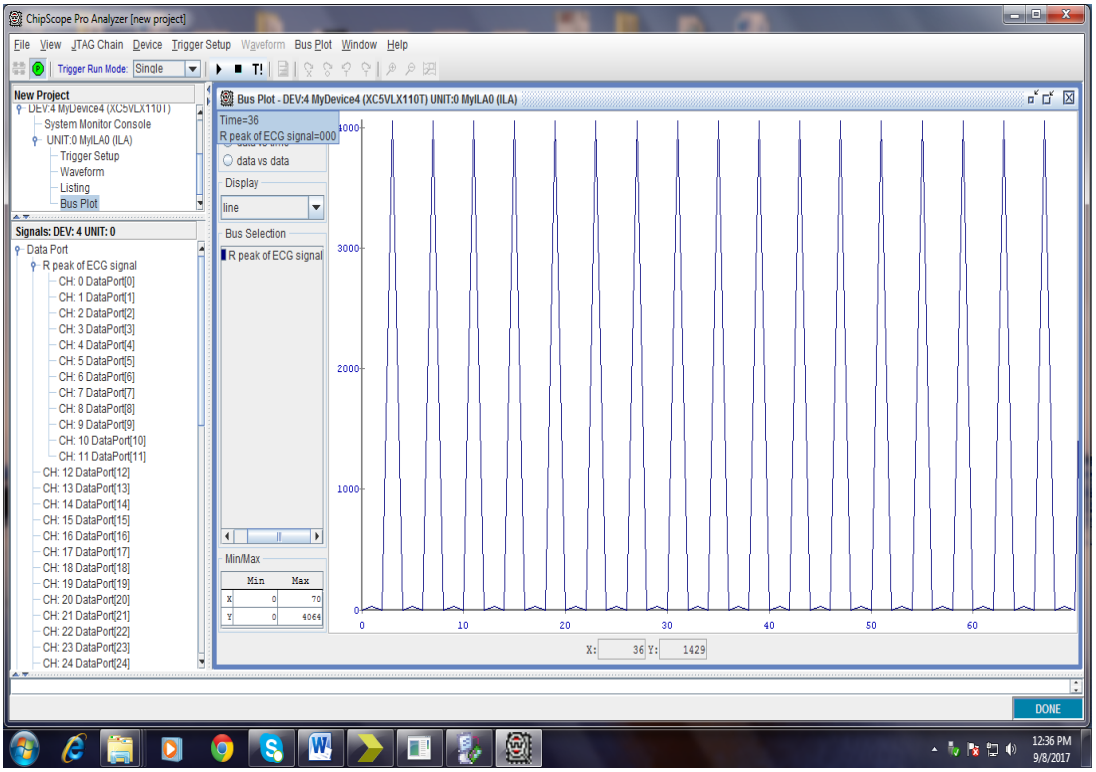


Fig.7.9 R peaks of ECG signal

The waveform suppressed the ‘P’ and ‘T’ waves and remains QRS wave shown the zoomed QRS complex signal is shown on fig. 7.9. Peak point on the Y-axis is the R- peak of the QRS complex wave by observing the signal on the bottom has 2 small peaks which are suppressed completely represents the ‘P’, and ‘T’ waves. The triangle is the QRS complex wave with peak being R- wave and left side is the ‘Q’ wave and right of ‘R’ peak is the ‘S’ wave. The heart beat of patient is calculated with the help of equation

$$Heart\ Rate = \left(\frac{Sampling\ Rate}{RR\ Interval\ in\ Samples}\right) \times 60$$

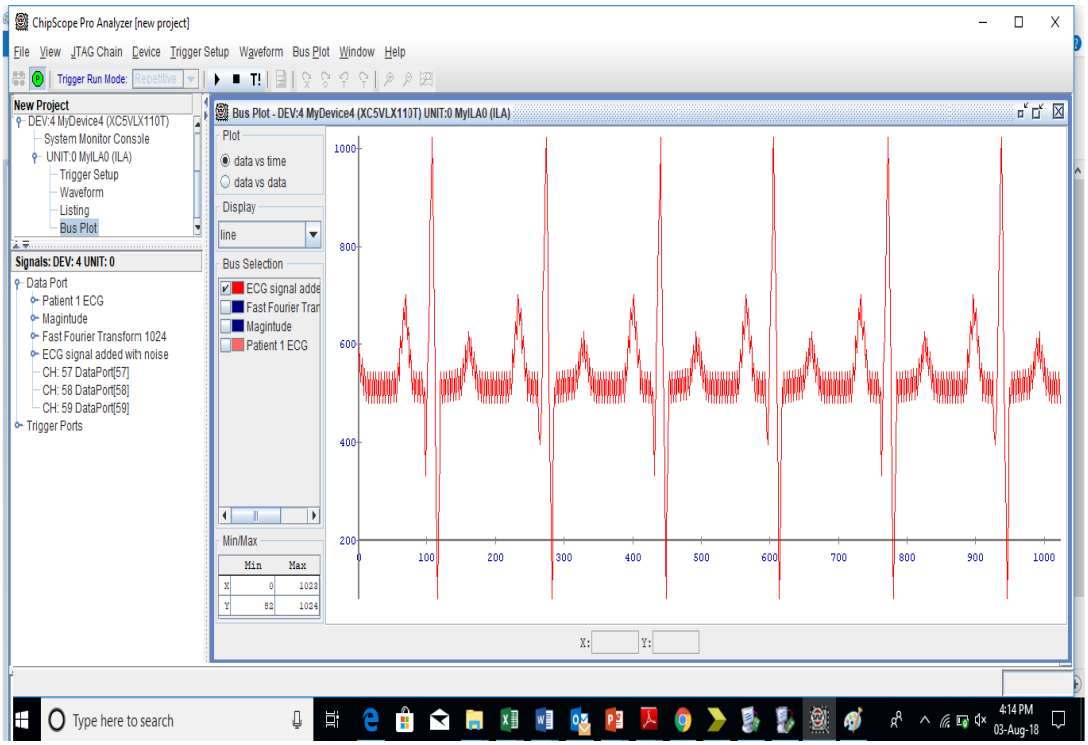


Fig.7.10 Chipscope analyzed ECG signal with noise

The fig. 7.10 is presents the ECG signal with noise in the chipscope pro analyzer the on chip verification the input to the signal is noise added to the signal and the noise is created by using the Direct digital synthesizer the DDS core in the Xilinx ISE.X-axis represents the time and Y-axis represents the amplitude of the ECG signal. The filtering techniques are used to remove the power frequency and the

bad pass filter is used to remove the high pass frequency that is beyond 100Hz and the low pass frequency below 0.05 Hz.

ECG signal after the filtering is shown in fig.7.11 which is the original ECG signal**.** All the time domain parameters are observing in the waveform. The first maximum peak in the waveform is ‘P’ wave. The second minimum in the waveform is ‘Q’ wave. The second maximum peak is ‘R’ wave. Second minimum is considered as ‘S’ wave and finally third maximum is ‘T’ wave. The waveform is periodic in nature and it is continuing on the chips cope until the FPGA is forcible stopped or in case of power failure.

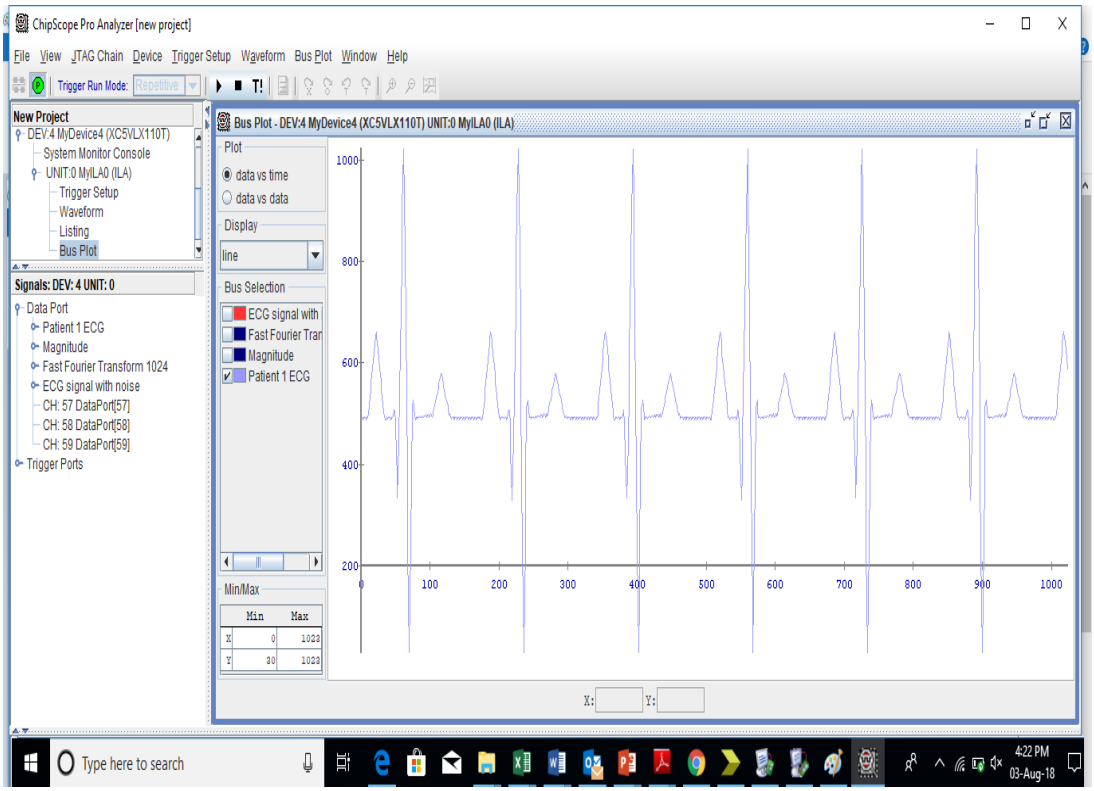


Fig.7.11 Chipscope analyzed ECG signal with noise removal (original)

The fig. 7.12 presents 1024 point FFT window running in FPGA as inbuilt synthesized core to process the ECG signal The ECG FFT output is the 1024-point FFT where X axix is the total number of point to calculate FFT starts at 0 index and completes at 1023 points. As filtered ECG signal is given to the FFT, the output is

analyzed in real and imaginary domain. To plot the FFT output, the signals needed to add real and imaginary part so magnitude signal is combined output of the real and imaginary part of the signals. The output of FFT is the double-sided band where there are two peaks observed (Output of FFT is symmetry) The first peak is at 5th index and one more peak is at the 1018th index is the maximum peak is observed for the dominant frequency

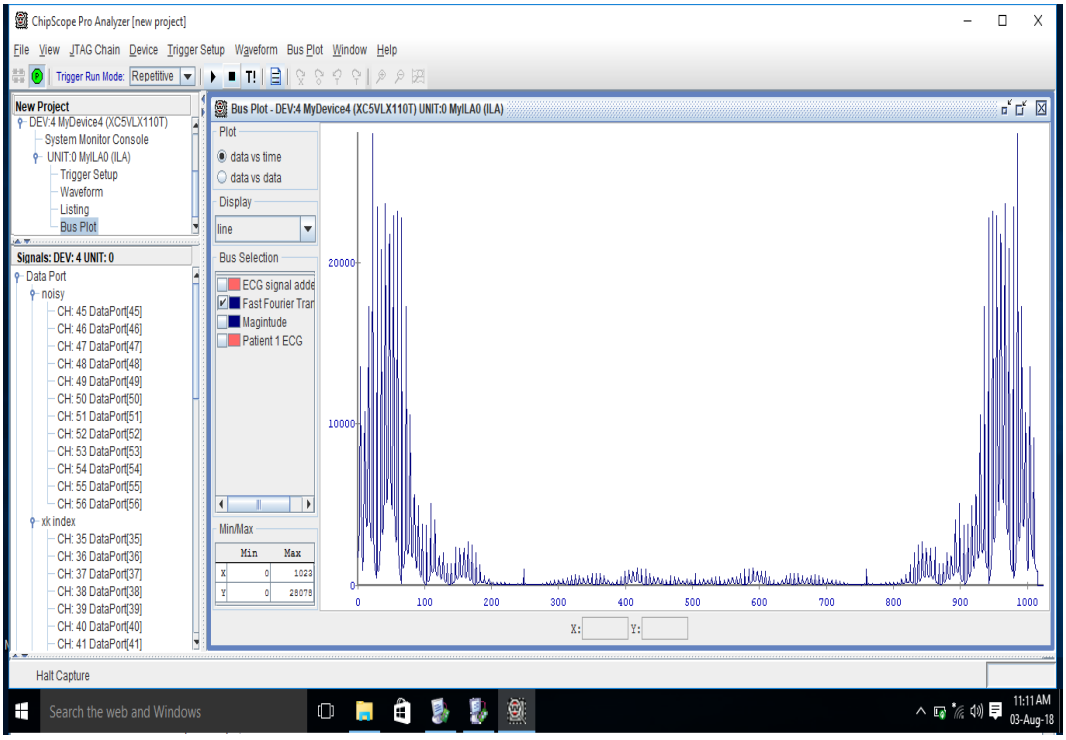


Fig.7.12 Chipscope analyzed 1024 point FFT window signal

Fig.7.13 is the zoomed FFT of the ECG signal at the beginning index points by monitoring the FFT output the experts can derive the condition of the patient. The frequency values for ‘P’ wave is 12.5Hz whose time domain value is 0.08Seconds. “QRS” complex frequency is 11 Hz and time domain value is 0.09 Seconds. The frequency values for ‘T’ wave is 6.25Hz and time domain value is 0.16 Seconds. The figure shown below has all the peaks up to 100 frequency.

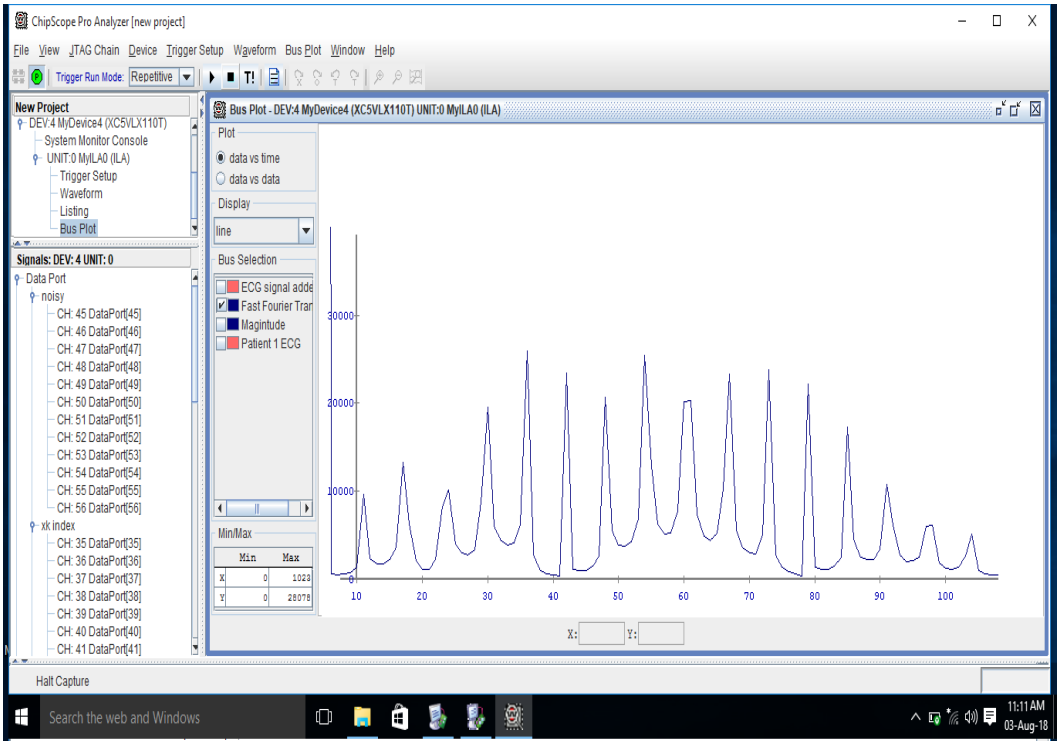


Fig.7.13 Zoomed FFT window signal

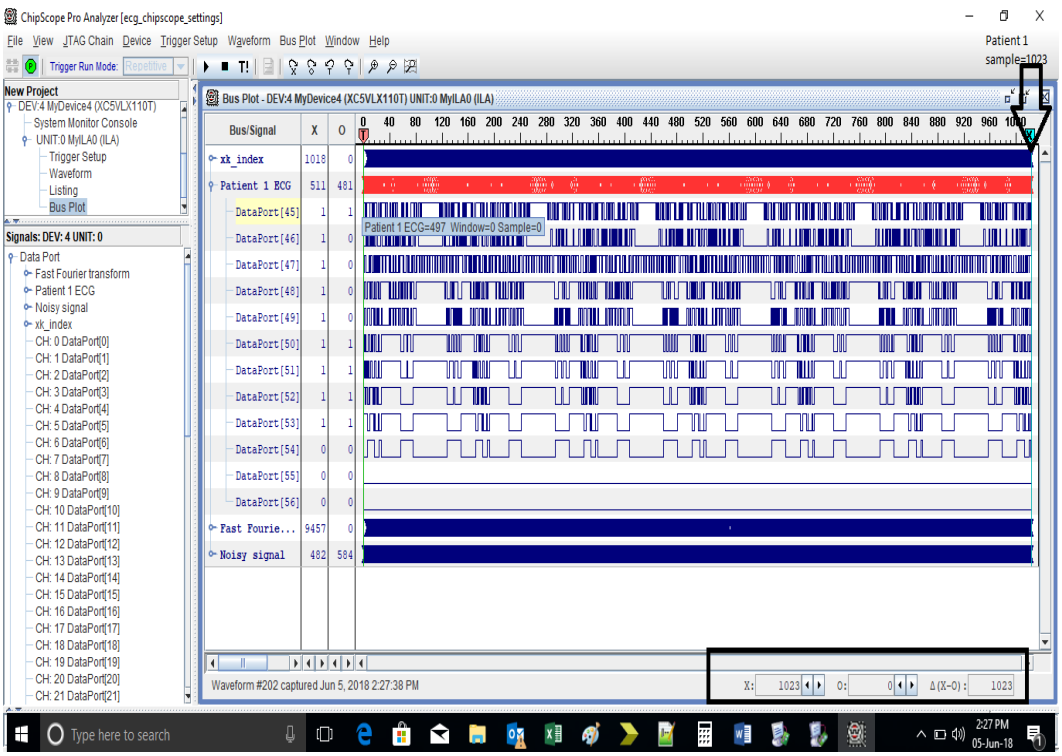


Fig.7.14 ECG R peak detection window under Chipscope analyzer

Fig.7.14 presents the ECG R- peak detection window under Chipscope analyzer to get the value for heat beat calculations. The waveform presents the internal signals of the ECG filtered signal for patient -1. Data port 45 to data port 56 is considered as the bus signal to the ECG filtered signal. Data port [45] to Data port [56]. The 12 bit data is "0001 1111 1111" which is equivalent to the decimal value 512. Table 7.2 list the heart rate of 30 patients and corresponding graph is depicted in fig. 7.15, obtained from the Xilinx simulator.

Table 7.2 Heart rate of 30 patients calculated form simulated waveform in Xilinx chipscope simulator

S. No.	**ECG sample collected from physionet.org database**	**Heart rate**	**Patient Heart Status**
Patient-1	Record ptbdb/patient001/s0014lre from 0:00.000 to 1:00.000	69	Normal
Patient-2	Record ptbdb/patient003/s0017lre from 0:00.000 to 1:00.000	102	Tachycardia
Patient-3	Record ptbdb/patient007/s0026lre (i) , from 0:00.000 to 1:00.000	72	Normal
Patient-4	Record ptbdb/patient035/s0145lre (ii) from 0:00.000 to 1:00.000	54	Bradycardia
Patient-5	Record ptbdb/patient067/s0230lre (iii) , from 0:00.000 to 1:00.000	75	Normal
Patient-6	Record ptbdb/patient180/s0545_re (avr) , from 0:00.000 to 1:00.000	115	Tachycardia
Patient-7	Record ptbdb/patient219/s0441_re (avr) , from 0:00.000 to 1:00.000	70	Normal
Patient-8	Record ptbdb/patient286/s0546_re , from 0:00.000 to 1:00.000	85	Normal

Patient-9	Record ptbdb/patient289/s0550_re , from 0:00.000 to 1:00.000	59	Bradycardia
Patient-10	Record ptbdb/patient294/s0559_re , from 0:00.000 to 1:00.000	69	Normal
Patient-11	record ptbdb/patient008/s0068lre , from 0:00.000 to 0:10.000record	73	Normal
Patient-12	Record ptbdb/patient009/s0035_re , from 0:00.000 to 0:10.000	90	Normal
Patient-13	Record ptbdb/patient010/s0036lre , from 0:00.000 to 0:10.000	68	Normal
Patient-14	Record ptbdb/patient011/s0049lre , from 0:00.000 to 0:10.000	67	Normal
Patient-15	Record ptbdb/patient012/s0050lre , from 0:00.000 to 0:10.000	54	Bradycardia
Patient-16	Record ptbdb/patient013/s0072lre , from 0:00.000 to 1:00.000	98	Normal
Patient-17	Record ptbdb/patient014/s0071lre , from 0:00.000 to 1:00.000	66	Normal
Patient-18	Record ptbdb/patient015/s0057lre , from 0:00.000 to 1:00.000	73	Normal
Patient-19	Record ptbdb/patient020/s0079lre , from 0:00.000 to 1:00.000	64	Normal
Patient-20	Record ptbdb/patient024/s0084lre , from 0:00.000 to 1:00.000	61	Normal
Patient-21	Record ptbdb/patient028/s0090lre , from 0:00.000 to 1:00.000	73	Normal
Patient-22	Record ptbdb/patient040/s0131lre , from 0:00.000 to 1:00.000	60	Normal
Patient-23	Record ptbdb/patient050/s0215lre , from 0:00.000 to 1:00.000	65	Normal

Patient-24	Record ptbdb/patient055/s0194lre , from 0:00.000 to 1:00.000	59	Bradycardia
Patient-25	Record ptbdb/patient065/s0229lre , from 0:00.000 to 1:00.000	68	Normal
Patient-26	Record ptbdb/patient070/s0235lre , from 0:00.000 to 1:00.000	101	Tachycardia
Patient-27	Record ptbdb/patient073/s0252lre , from 0:00.000 to 1:00.000	68	Normal
Patient-28	Record ptbdb/patient080/s0261lre , from 0:00.000 to 1:00.000	68	Normal
Patient-29	Record ptbdb/patient105/s0303lre , from 0:00.000 to 1:00.000	70	Normal
Patient-30	Record ptbdb/patient215/s0437_re , from 0:00.000 to 0:10.000	74	Normal

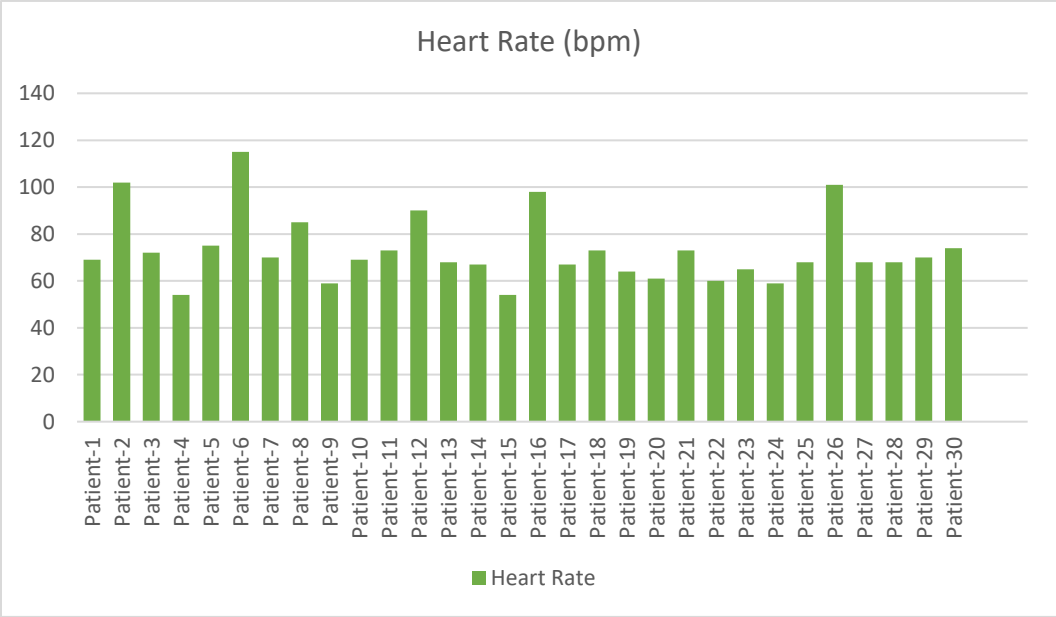


Fig. 7.15 Heart beat variation graph for different patients obtained from Xilinx Chipscope Pro-Analyzer waveform

The analysis of the heart rate is done based on the 'z' statistics test. Table 7.3 Calculation for the statistical analysis of the heart rate. The equation used of to calculate the value of 'z' is given as

$$z = \frac{\bar{X} - \mu_{H0}}{SE} = \frac{X - \mu_{H0}}{\sigma_p/\sqrt{n}} \quad (7.6)$$

Where,

$$\sigma_p = \sqrt{\frac{\sum(X_i - \bar{X})^2}{n}} \quad (7.7)$$

$$\bar{X} = \frac{x_1 + x_2 \ldots\ldots\ldots\ldots\ldots x_n}{n} \quad (7.8)$$

Here, $\bar{X}$ = μ = mean of sample

μ_{H0} = mean of the population

σ_p = standard deviation of the population

n = no. of observations

Let us assume that null hypothesis $H_0 = \mu_{H0} = 72$ and

Alternate Hypothesis $H_a = \mu_{H0} \neq 72$

Table 7.3 Calculation for the statistical analysis of the heart rate

S. No.	$\mathbf{X_i}$	$(\boldsymbol{X_i - \bar{X}})$	$(\boldsymbol{X_i - \bar{X}})^2$
Patient-1	69	-3	9
Patient-2	102	30	900
Patient-3	72	0	0
Patient-4	54	-18	324
Patient-5	75	3	9
Patient-6	115	43	849
Patient-7	70	-2	4

Patient-8	85	13	169
Patient-9	59	-13	169
Patient-10	69	-3	9
Patient-11	73	1	1
Patient-12	90	18	324
Patient-13	68	-4	4
Patient-14	67	-5	25
Patient-15	54	-18	324
Patient-16	98	26	676
Patient-17	66	-6	36
Patient-18	73	1	1
Patient-19	64	-8	64
Patient-20	61	-11	121
Patient-21	73	1	1
Patient-22	60	-12	144
Patient-23	65	-7	49
Patient-24	59	-13	169
Patient-25	68	-4	16
Patient-26	101	29	841
Patient-27	68	-4	16
Patient-28	68	-4	16
Patient-29	70	-2	4
Patient-30	74	2	4
	$\boldsymbol{\bar{X} = 73}$	$\boldsymbol{\sum(X_i - \bar{X}) = 30}$	$\boldsymbol{\sum(X_i - \bar{X})^2 = 6290}$

$$\sigma_p = \sqrt{\frac{\sum(X_i - \bar{X})^2}{n}} = \sqrt{\frac{6290}{30}} = 14.47$$

Standard Error,

$$SE = \frac{\sigma_p}{\sqrt{n}} = \frac{14.47}{\sqrt{30}} = 2.64$$

$$z = \frac{\bar{X} - \mu_{H0}}{SE} = \frac{(73 - 72)}{2.64} = \frac{1}{2.64} = 0.378$$

The value of z is 0.378 and applying the two-tailed test for determining the rejection regions at 5 % level of significance, which comes to under using normal curve followed for Z area table

$$R: |z| > 1.96$$

Hence, our hypothesis $H_0 = \mu_{H0} = 72$ is accepted to estimate that the mean is consistent with the population mean and population mean is supporting to our results. The value $z = 0.378$ provides the positive results to support our Chipscope Analyzer based analysis of FPGA and Modelsim simulation.

7.4 FPGA Device Utilization Summary

The FPGA device utilization summary is directly taken form Xilinx ISE 14.2. The report consist of the information of no. of slice register, no. of slices, no. of LUTs. No. of flip-flops/ Latches, No. of DSP blocks, memory utilization , Shift registers input/ output blocks/(IOBs), RAM Modules with blocked RAM and FIFO and no of buffers etc. The information is used to estimate the hardware resources utilization of FPGA for synthesis. If the resources utilization is greater than 100 %, then the designer has to change the design to synthesis on same FPGA. Table 7.4 list the detail of the hardware resources utilized on Virtex -5 FPGA for pre-synthesized code.The timing values of the same FPGA is listed in table 7.5. The table presents the details of the timing information such as minimum period, minimum and maximum time of arrival before and after clock signal, combinational path delay. The table also list the information of the maximum frequency support for the configured FPGA device.

Table 7.4 Hardware utilization detail on FPGA

Hardware Parameter	**Used**	**Available**	**Utilization**
Number of Slice Registers	523	69,120	1%
Number of Slice LUTs	450	69,120	1%
Number used as logic	320	69,120	1%
Number used as Memory/Shift register	97	17,920	1%
Number of occupied Slices	262	17,280	1%
Number with an unused Flip Flop	157	680	23%
Number with an unused LUT	230	680	33%
Number of fully used LUT-FF pairs	293	680	43%
Number of slice register sites lost to control set restrictions	127	69,120	1%
Number of bonded IOBs	23	640	1%
Number of LOCed IOBs	2	23	1%
Number of Block RAM/FIFO	2	148	1%
Total Memory used (KB)	72	5,328	1%
Number of BUFG/BUFGCTRLs	4	32	12%
Number of BSCANs	1	4	25%
Number of DSP48Es	4	64	6%

Table 7.5 The Timing Values for configured devices on Virtex-5 FPGA

Timing Parameter	**Utilization**
Max Frequency	714.461Mhz
Minimum Period	8.100 ns
Time before clk (minimum)	7.128 ns
Time after clock (maximum)	6.518 ns
Combinational Path delay	3.592 ns
Speed Grade	-5

7.5 Comparative Analysis

The comparative analysis is also done for the same configured ECG processing unit. The device utilization and timing analysis is also don on SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA. Table 7.6 presents the comparative hardware utilization to support the same functionality of the chip.

Table 7.6 Hardware utilization detail on FPGA

Hardware Parameter	**SPARTAN-3E**	**SPARTAN-6**	**Virtex-5**
Number of Slices	1449	1438	523
Number of Slice LUTs	1263	1104	450
Number used as logic	1193	829	320
Number used as Memory/Shift register	311	174	97
Number of occupied Slices	1193	508	262
Number with an unused Flip Flop	567	298	157
Number with an unused LUT	438	384	230
Number of fully used LUT-FF pairs	1204	806	293
Number of slice register sites lost to control set restrictions	417	370	127
Number of bonded IOBs	23	23	23
Number of Locked IOBs	3	3	2
Number of Block RAM/FIFO	9	8	2
Total Memory used (KB)	4447828 KB	4526620 KB	4687396 KB
Number of BUFG/BUFGCTRLs	4	4	4
Number of BSCANs	1	1	1
Number of DSP48Es	0	8	4

Fig. 7.16 presents the comparative graph to support the hardware utilization of the FPGA parameters number of Slices, number of Slice LUTs, number used as logic, number used as memory/shift register, number of occupied Slices, number with an unused flip-flop, number with an unused LUT, number of fully used LUT-FF pairs and number of slice register sites lost to control set restrictions. The graph depicts that the hardware utilization in Virtex-5 is very much less in comparison to the hardware utilization on SPARTAN-6 and SPARTAN-3E.

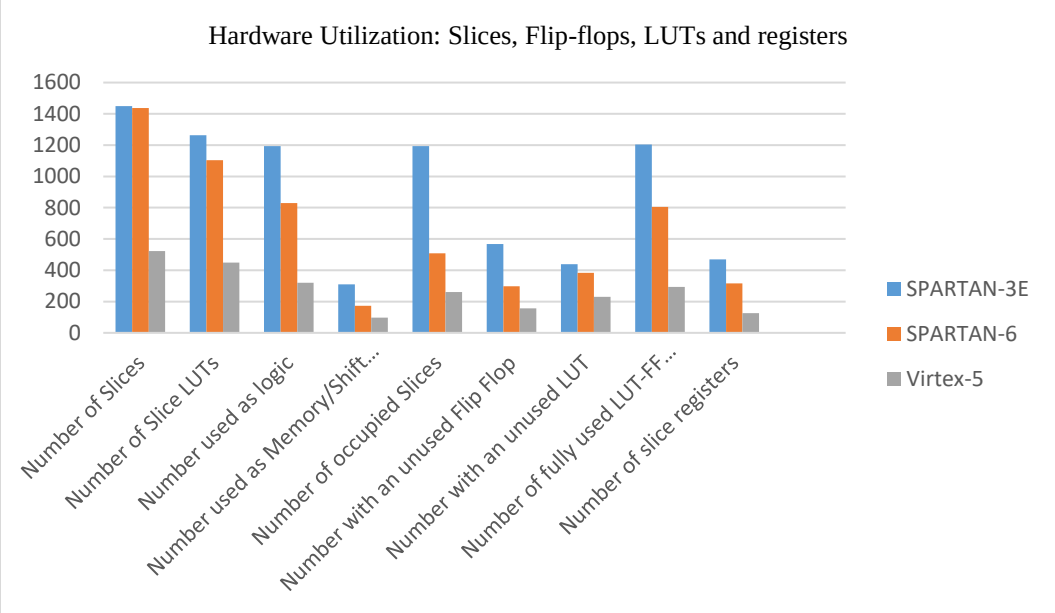


Fig. 7.16 Comparative graph for Hardware Utilization: Slices, Flip-flops, LUTs and registers

In the same way, Fig. 7.17 presents the comparative graph to support the hardware utilization of the FPGA parameters: number of bounded IOBs, number of Locked IOBs, number of Block RAM/FIFO logic, number pf BUFG/BUFGCTRLS, number of BSCANs and number DSP elements. The graph depicts that the hardware utilization of IOBs, RAM/FIFO, DSP elements etc is very much less in comparison to the hardware utilization on SPARTAN-6 and SPARTAN-3E. The hardware results estimate that Virtex-5 provides the optimized hardware resources utilization for developed chip.

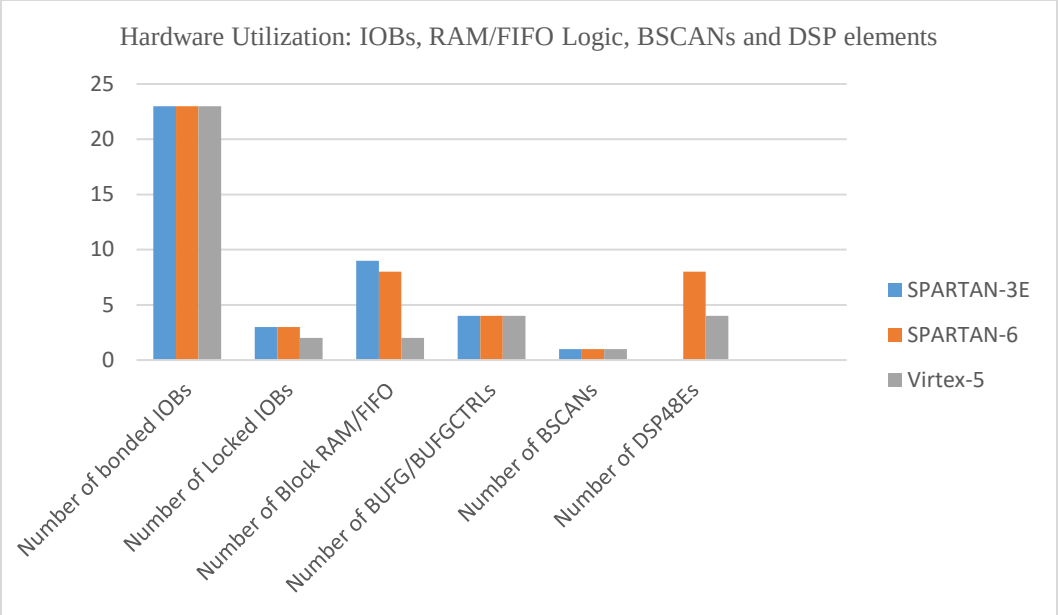


Fig. 7.17 Comparative graph for Hardware Utilization: IOBs, RAM/FIFO Logic, BSCANs and DSP elements

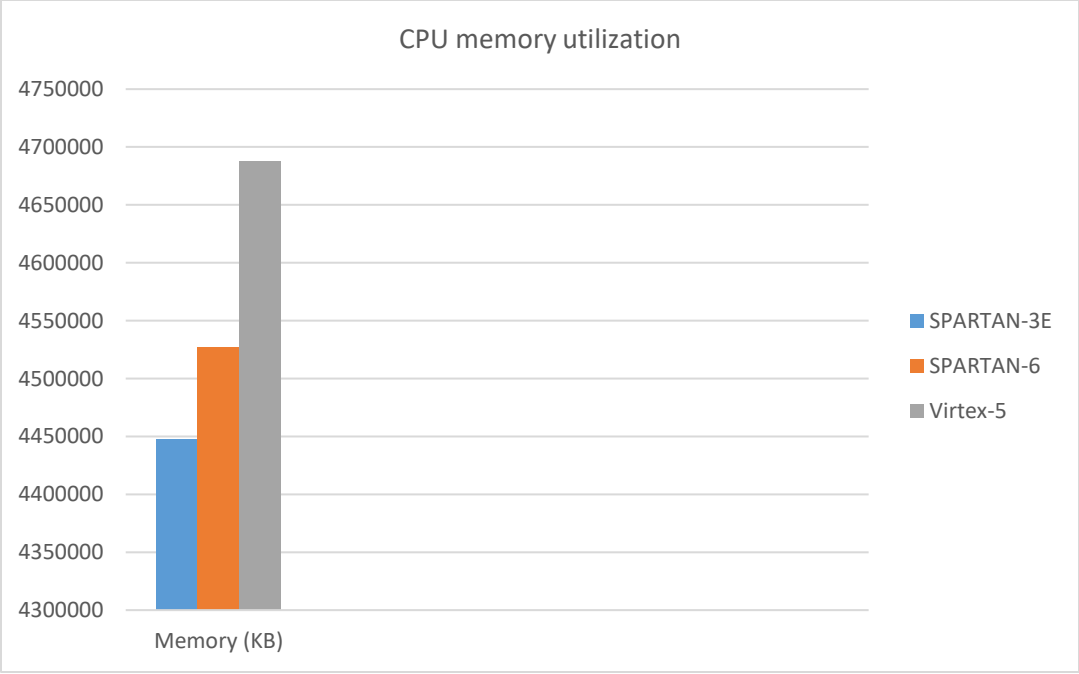


Fig. 7.18 Comparative graph for CPU memory utilization

The CPU memory utilization graph is shown in fig. 7.18, in which it is depicted that the memory utilization of Virtex-5 device on CPU is more because the inbuilt hardware support of the FPGA is more in compassion to SPARTAN 3E and SPARTAN 6. The table 7.7 presents the comparative timing information of the same chip against the timing parameters such as minimum period, minimum and maximum time before and after the clock , total delay , maximum frequency support for SPARTAN 3E, SPARTAN 6 and Virtex -5 FPGA. The comparative graph for the time is depicted in in fig 7.19 and frequency support graph in fig. 7.20.

Table 7.7 The timing values for configured devices on Virtex-5 FPGA

Timing Parameter	**SPARTAN-3E**	**SPARTAN-6**	**Virtex-5**
Max Frequency	359.120 MHz	507.389 MHz	714.461MHz
Minimum Period	16.915 ns	9.312 ns	8.100 ns
Time before clk (minimum)	16.452 ns	9.094 ns	7.128 ns
Time after clock (maximum)	11.930 ns	7.804 ns	6.518 ns
Combinational Path delay	7.846 ns	4.330 ns	3.592 ns
Speed Grade	-5	-5	-5

The value of minimum period is 16.915 ns, 9.312 ns and 8.100 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. In the same way the values of min time before clock signal is 16.452 ns, 9.094 ns and 7.128 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. Maximum time after clock signal is 11.930 ns, 7.804 ns and 6.518 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. The combinational path delay is 7.846 ns, 4.330 ns and 3.592 ns for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively. The timing results for Virtex-5 FPGA are optimized in comparison to SPARTAN -3E and SPARTAN-6 FPGA. The value of maximum frequency support is 359.120 MHz, 507.389 MHz and 714.462 MHz for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA respectively.

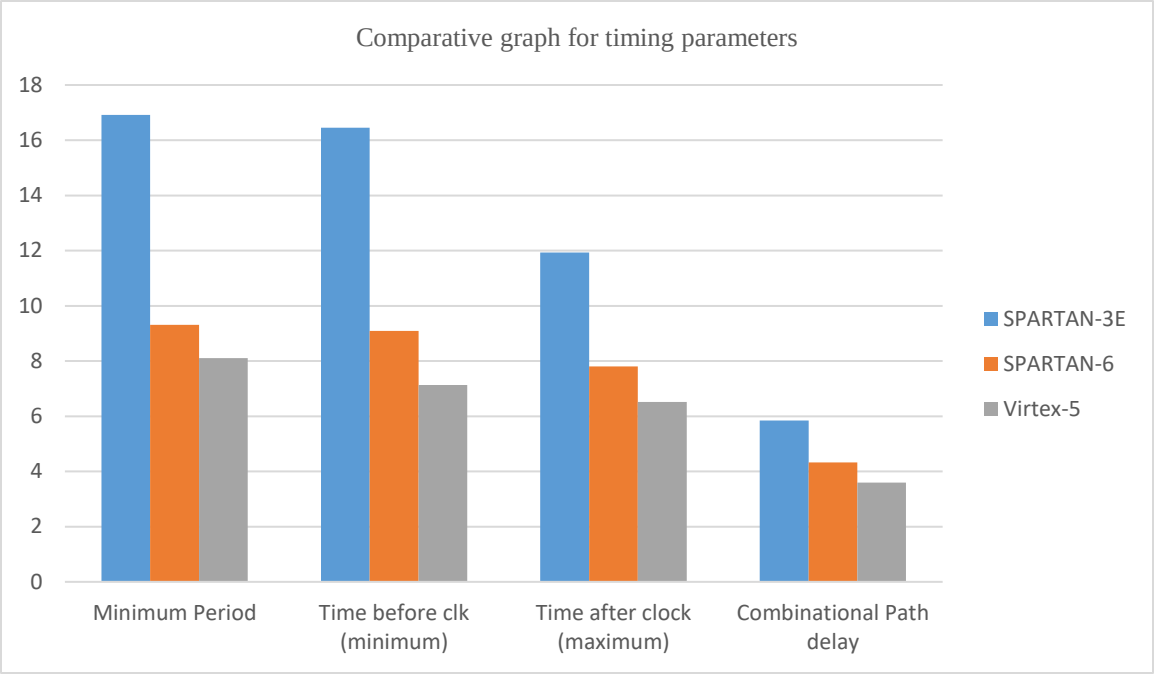


Fig. 7.19 Comparative timing analysis for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA

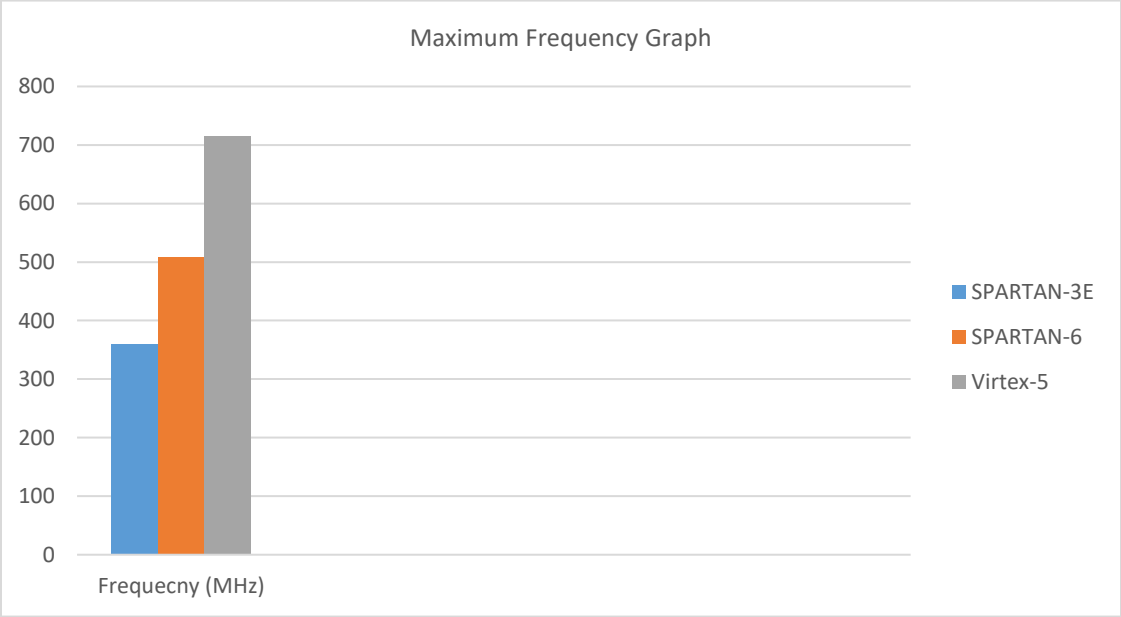


Fig. 7.20 Comparative analysis of maximum frequency support for SPARTAN-3E, SPARTAN-6 and Virtex-5 FPGA

The Virtex-5 supports the maximum frequency in comparison to SPARTAN 3E and SPARTAN-6, which signifies that the Virtex-5 is much faster. The minimum timing values, hardware support parameters and frequency support results estimates that Virtex-5 FPGA is the optimal solution in comparison to other FPGA. Table 7.8 presents the comparative analysis of the synthesized results of Virtex-5 FPGA with existing research work.

Table 7.8 Comparison with existing work

Parameters	**Jatmiko et al (2011)**	**D.Panigraphy et al (2015)**	**M.G Egila et al (2016)**	**T.H. Lu et al (2016)**	**M.A Kumar et al (2018)**	**Our Work Virtex-5**
No. of slice registers	7301	5728	3893	966	1086	512
No. of slice LUTs	7654	88456	3953	842	1408	450
No. of Fully used LUTs, FF pairs	8832	188	4321	458	1052	293
No. of Bounded IoBs	14	114	140	46	82	23
No. of BUFGs	4	1	4	1	2	4

The comparative analysis of the existing work with our work revels that the hardware parameters utilization of our work is less in comparison to the work done by Jatmiko et al (2011), D.Panigraphy et al (2015), M.G Egila et al (2016), T.H. Lu et al (2016) and M.A Kumar et al (2018). The No. of slices, No. of slice LUTs, No. of Fully used LUTs, FF pairs, No. of Bounded IoBs and No. of BUFGs on Virtex-5 are 512, 450, 293, 23 and 4 respectively. The results are optimal in terms of hardware parameters synthesized on FPGA.

CHAPTER-8
CONCLUSION

The chapter presents the conclusions drawn from the research work and recommendations about the further research and possibilities

8.1 Conclusions

Most of the cardiovascular diseases including heart disease depends on the heart functioning. There are some techniques and electronic systems to prevent heart attacks, heart stokes and related diseases of heart. The ECG is the technology that provides electrical behavior of heartbeat by an impulse wave in heart to the muscle to squeeze and pumping blood into heart. The left and right atria make the first wave called 'P' wave or upper chambers wave followed by flat line to bottom chambers. The left and right ventricles creates the next wave as QRS complex followed by electrical recovery 'T' wave. The ECG machine records the ECG signal and doctors makes their decision based on the ECG signal characteristics. The high speed and fast response system are the demand of future electronics system. The ECG electronics system has ADC module, ADC interface module, power line noise removal, high frequency noise removal filter, dual port RAM, and FFT, magnitude and phase analyzer.

- In the research work, the chip design of the individual module and its integration as top-level chip and schematic is done successfully in Xilinx ISE 14.2 software.
- The proposed design and implementation and verification of the ECG system chip to monitor the heart rate for high response electronic hardware embedded with the FPGA the ECG system consists have 3 leads to monitor the positions of human Right arm, Left Arm, Right Leg or Left leg.

- The functional simulation of individual module and integrated ECG chip is carried out in Modelsim 10.0 with several test cases.
- The code design is carried with different optimization technique and adoption of the filter.
- The MATLAB Filter design tool is used for the noise removal of power line interference with the notch filter. High pass noise removal filter with the FIR band pass equiripple filter.
- The parallel and pipelined architecture of FFT is carried to make system faster based on inbuilt 1024 point FFT IP core.
- The patient data is taken from the MIT-BIH database. The MATLAB simulation is carried for 30 sampled patients to get the ECG simulation waveform, and further analysis of heartbeat to estimate the accuracy of MATLAB based system using 'Z' test.
- The same data to MIT – BIH is carried on FPGA based high performance ECG chip system to analyze the heart beat and estimation of the system accuracy using 'Z' test.

The hardware parameters such as number of slices, number of slice LUTs, number of fully used LUTs, FF pairs, number of bounded IoBs and number of BUFGs are analyzed directly from Xilinx software to understand the hardware utilization. In same with timing parameters such as minimum period, minimum and maximum time before and after the clock, total delay , are utilized to understand the system response.

- The chip Verification and synthesis is carried on SPARTAN 3E, SPARTN-6 and Virtex-5 FPGA to estimate the system performance is optimal on Virtex 5 FPGA in terms of hardware, memory and timing parameters.
- The timing information such as minimum period, minimum and maximum time of arrival before and after clock signal, and combinational path delay is 8.100 ns, 7.128 ns, 6.518 ns and 3.592 ns respectively. The maximum frequency support for the configured FPGA device is 714.461MHz.

- The design and FPGA parameters are compared with SPARTAN-3E, SPARTA-6 and Virex-5 FPGA to understand the real time ECG signal processing in Virtex 5 FPGA gives the optimal solution in terms of timing parameters.
- The internal signal of the ECG chip is analyzed on Chipscope Pro- Analyzer successfully for the all test cases.
- The comparative analysis of the existing work with our work is done successfully. The hardware parameters utilization of our work is less in comparison to the work done by Jatmiko et al (2011), D. Panigraphy et al (2015), M.G Egila et al (2016), T.H. Lu et al (2016) and M.A Kumar et al (2018).
- The No. of slices, No. of slice LUTs, No. of Fully used LUTs, FF pairs, No. of Bounded IoBs and No. of BUFGs on Virtex-5 are 512, 450, 293, 23 and 4 respectively. The results are optimal in terms of hardware parameters synthesized on FPGA.
- The FPGA integration and real time integration of electrodes with human body experimental set up shows the live heart bet detection on the LCD display of same FPGA.

8.2 Future Work

The proposed system is the boon for the industries working on the high performance ECG system integration with programmable devices. The future cardiac system need have the requirement of multi patient operation with higher throughput and lesser delay. In recent time, remote ECG monitoring systems have been functional in the monitoring of numerous kinds of heart diseases, and the superiority of ECG signal transmission and reception for remote process is kept advancing. The wearable health system are based on microprocessor-based system helpful for customized solution for body area network, smart textiles, mobile phone and commercial Bluetooth sensor etc. The wearable systems used in real time clinical applications have numerous of challenges needed to be addressed including signal

correlation, sensor contact, rotation, location, and patient comfort, and multiple objective functions including functionality and wearability . The design and implementation of MEMS based wearable ECG chip for patients will be the future research. Our developed chip, design can be integrated and synthesized on recently launched Virtex-7 highest performance and integration at 28 nm and Intel's Stratix® 10 on 14 nm FPGA.

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APPENDIX-A

Publications

1. **B. Khaleelu Rehman**, Adesh Kumar, Paawan Sharma, "A Novel approach for R- Peak detection in the Electrocardiogram(ECG) signal**"** *ARPN Journal of Engineering and Applied Science(JEAS) ,December 2016,*Volume 11 number 21 , Page(s): 13500 – 13503,ISSN-1819-6608. **(Scopus Indexed)**

2. **B. Khaleelu Rehman**, Adesh Kumar, and Paawan Sharma "Comparative study of high performance QRS complex detection on Electrocardiogram signal ".*International Journal of control theory and applications(IJCTA)*. Volume: No.10 (2017) Issue No. **:** 7 (2017).Pages 111-120. **ISSN:** 0974-5572. **(Scopus Indexed)**

3. **B. Khaleelu Rehman**, Adesh Kumar, and Paawan Sharma "A FPGA based High performance heart beat monitoring system". *International Journal of control theory and applications (IJCTA*). Volume: No.10 (2017) Issue No. **:** 18 (2017).Pages 245-253. ISSN: 0974-5572. **(Scopus Indexed)**

4. **B. Khaleelu Rehman**, Adesh Kumar, and Paawan Sharma. "Modeling and Simulation of ECG Signal for Heartbeat Application. "Advances in *Intelligent Communication, Control and Devices*, pp. 503-511. Springer, Singapore, 2018. **(Scopus Indexed)**

Curriculum Vitae

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SUMMARY

1. Pursuing Ph.D in VLSI DESIGN from the UPES,Dehradun

2. Completed **M.Tech (VLSI)** with 10 years of teaching experience in various subjects of Electronics and Communication Engineering.

3. Present a paper in international conference on DTMF detection by using Goertzal algorithm, a resource sharing approach.

4. Organized a 2 day workshop in UPES on "Digital signal processing and its applications" on Nov 2012.

Work Experience

1 Worked as an Asst. Prof. in Dept. of ECE at **Avanthi Institute of Engineering and Technology**, Hayatnagar, Hyderabad from **April 2008 to Nov 2010**.

2 Worked as an Asst. Prof. in Dept. of ECE at **Kommuri Pratap Reddy Institute Of Tecnolgy, Ghatkesar,Hyderabad** from **Nov 2010 to Dec 2011**.

3 Working as Asst. Prof. in Dept. of EE&I **at University Of Petroleum And Energy Studies(UPES),** Bidholi, Dehradun from **Jan 2012 to till date**

Publication details

International Journals

1.B.Khaleelu Rehman ,Adesh kumar, Paawan Sharma, "A Novel approach for R-Peak detection in the Electrocardiogram(ECG) signal" ARPN Journal of Engineering and Applied Science(JEAS) ,December 2016,Volume 11 number 21 , Page(s): 13500 – 13503,ISSN-1819-6608.

2.B.Khaleelu Rehman, Adesh kumar,Paawan Sharma "Comparative study of high performance QRS complex detection on Electrocardiogram signal ".International Journal of control theory and applications(IJCTA). **Volume:** No.10 (2017) **Issue No. :** 7 (2017).Pages 111-120. **ISSN:** 0974-5572.

3. Sana parween, Madhurima, B.Khaleelu Rehman "A Novelty techniques for noise removal in ECG signals"International Journal of Electrical,Electronics & Compter Science Engineering (E2CE-2016), 2016 12-13 August 2016 , Page(s): 14 – 16,Specail issue Print ISBN: 2454-1222, Online ISBN:2348-2237.

4. Adesh Kumar, Gaurav Verma, Mukul Kumar Gupta, Mohammad Salauddin, BeporamKhaleelu Rehman, Deepak Kumar "3D Multilayer Mesh NoC Communication and FPGASynthesis" Wireless Personal Communications.

5.Shubhankar Thapliyal , Kartik Sehgal , Utkarsh Sundaram, Akshay Sharma , B Khaleelu Rehman "Designing an Improved 64 Bit Arithmetic and Logical Unit for Digital Signaling Processing Purposes" International Scientific Research Organization Journal, Volume 02 Issue 01, 2017, e-ISSN- 2455–8818.

International Conferences

1. B.Khaleelu Rehman ,Venkata siva reddy,P.vishnu kumar,K.maheswari, "Design and verification of 16 bit Vedic multiplier using 3:2 compressors and 4-Bit novel adder"

2. International Conference on Intelligent Communication, Control and Devices (ICICCD-2016),page(s):723-732, Print ISBN: 978-981-10-1708-7, Online ISBN: 978-981-10-1708-7.

3. Iftekhar Hussain,Mirsafiuall,B.khaleelu Rehman "Application of Rapid Tooling for vacuum forming to reduce cycle time". Presented a paper on "International Conference on Advances in the Field of Health, Safety, Fire, Environment, Allied Sciences and Engineering (HSFEA 2016)".

4. B.Khaleelu Rehman ,Sana parween, Madhurima, "A Novelty techniques for noise removal in ECG signals" International Conference on Advancement in Electrical, Electronics & Computer Engineering (E2CE-2016), 2016 12-13 August 2016 , Page(s): 14 – 16,Specail issue Print ISBN: 2454-1222, Online ISBN:2348-2237.

5. B.Khaleelu Rehman, Adesh kumar,Paawan Sharma "A FPGA based high performance heart beat monitoring system" International Conference on sustainable computing techniques in Engineering Science and management(SCESM-2017).

6. B.Khaleelu Rehman, Adesh kumar, Paawan Sharma "Modelling and simulation of ECG signal for heart beat application". Accepted a paper on International Conference on Intelligent Communication, Control and Devices (ICICCD-2017).

7. Mohammad Salauddin, Madan Gopal, Manda Rajarao,B. Khaleelu Rehman "Mitigation of Signal Interference by positioning FFT window for OFDMA system" Accepted a paper on International Conference on Intelligent Communication, Control and Devices (ICICCD-2017).

8. Mudasar Basha, M Siva Kumar, Vemulapalli Sai Pranav , B Khaleelu Rehman" approach to find shortest path using ant colony optimization (aco) in xilinx" Accepted a paper on International Conference on Intelligent Communication, Control and Devices (ICICCD-2017).

Subjects Handled

1. **VLSI Design** for III year ECE.
2. **Data Communication Systems** for III yr CSE.
3. **Signal processing** for M.Tech AI&ANN
4. **Digital Logic Design** for II yr CSE
5. **Digital Signal Processing** for III yr ECE.
6. **Electromagnetic Waves & Transmission Lines** for II yr ECE
7. **Probability theory and stochastic process** for II yr ECE
8. **Signals and Systems** for III SEM EE.
9. **Electronic Devices & Circuits** for IV SEM EE

Subjects taught for GATE coaching

Digital Signal Processing

Signals and Systems

Digital electronics

Labs Handled

1. **DSPLab** for III B.Tech ECE (using CC STUDIO & MATLAB)
2. **AC Lab** for II B.Tech ECE
3. **ECA Lab** for II B.Tech ECE
4. **PDC Lab** for II B.Tech ECE

SOFTWARE SKILL SET

Hardware descriptive Language : **VHDL, VERILOG**

Languages **:** **MATLAB**, **C**, **CPP**

ECE related software's

VLSI: CADENCE TOOLS, NC SIM, MODELSIM, XILINX'S, ACTIVE VHDL, MICROWIND.

DSP : CODE COMPOSER STUDIO, MATLAB.

EMBEDED SYSTEMS: KEIL.

P SPICE LAB: MULTISIM.

EDUCATIONAL PROFILE:

Course	Institution/ University	Year	%	Division
M.Tech (VLSI)	Shadaan College of Engg. and Tech., Hyderabad/JNTUH	2011	74	FIRST CLASS-Distinction
B.Tech (E.C.E)	Safa College of Engg. &Tech., Kurnool/ JNTU	2008	62	FIRST CLASS
Intermediate	Sree Manik Jr. College, Kurnool/ BIE, Hyd	2004	68	FIRST CLASS
S.S.C	Sree Manik High School, Kurnool/ BSE, Hyd	2002	74	FIRST CLASS

Personal Details

Name : B.KHALEELU REHMAN

Date of Birth : 11-08-1987

Father's name : B.RAFIQ AHAMED

Gender :Male

Marital Status : Married

Languages known : English, Hindi,Telugu,Urdu.

Permanent address : B.khaleelu Rehman, H.No: 51/15A-49-2C, Baba Brindavan Nagar, Behind 4th Town Police Station, Kurnool-518003,A.P.9985537956

DECLARATION:

I hereby declare that the information furnished above is true to the best of my knowledge.

Date:

Place: Dehradun

(B.KHALEELU REHMAN)