

Name:	 UPES UNIVERSITY WITH A PURPOSE
Enrolment No:	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, May 2019

Course: VLSI Design
Program: B.TECH EE spz BCT
Course Code: ELEG 407

Semester: VI
Time 03 hrs.
Max. Marks: 100

Instructions:

SECTION A 20Marks
All questions are compulsory

S. No.		Marks	CO
Q 1	Discuss the steps involved in the twin tub process	4M	CO1
Q 2	Demonstrate the CMOS inverter circuit	4M	CO2
Q 3	Explain pass transistor	4M	CO3
Q 4	Clearly explain each step of high level design flow of an ASIC.	4M	CO4
Q 5	Implement the VHDL code to perform 2's complement of a 4 bit binary number	4M	CO1

SECTION B 40 Marks

Each Question Carries 10 Marks Note: Attempt any one question from Qno 9

Q 6	Determine pull-up to pull-down ratio of an NMOS inverter when driven through one or more pass transistors.	10M	CO2
Q 7	What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for the logic $Y = (AB+C)'$ using CMOS	10M	CO3
Q 8	Explain about configurable FPGA based I/O blocks	10M	CO4
Q 9	(a) With neat sketches explain BICMOS fabrication in an p-well process (or) (b) Explain 4:1 multiplexer using the transmission gate and tristate inverter	10M	CO1 & CO3

SECTION-C 40Marks

Each Question Carries 20 Marks Note: Qno 10 is compulsory attempt any one question from Qno 11 & Qno 12

Q 10	(a) Write a VHDL code for BCD to seven-segment display converter using behavioral style of modeling. (b) For a CMOS inverter, calculate the shift in the transfer Characteristics curve when β_n / β_p ration is varied from 1/1 to 10/1	[10+10]	CO4 & CO2
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Q 11	Carry out the design of a 4 bit CMOS carry look ahead adder up to stick diagram form. Then determine what standard cells are needed and design a mask layout of each.	20M	CO3
Q 12	<p>(a) An n MOS transistor is operating in saturation region with the following parameters. $V_{gs}=7V$, $V_{th}=1.9V$, $(W/L) = 20$: $\mu_n c_{ox} = 130\mu A/V$ Find I_D and R_{DS}.</p> <p>(b) Explain $2\mu m$ Double Metal, Double Poly. CMOS / BiCMOS Rules.</p>	[10+10]	CO1 & CO2

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SECTION A 20Marks
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S. No.		Marks	CO
Q 1	Explain VLSI Design flow	4M	CO1
Q 2	Demonstrate the NMOS inverter circuit	4M	CO2
Q 3	Write a VHDL code to implement 4 bit parallel adder circuit	4M	CO3
Q 4	Draw the pass transistor arrangement for the logic $Y=ABC$	4M	CO4
Q 5	Discuss the four generations of Integrated circuits with examples	4M	CO3

SECTION B 40 Marks

Each Question Carries 10 Marks Note: Attempt any one question from Qno 8

Q 6	Distinguish PLAs, PALs, CPLDs, FPGAs and standard cells in all respects	10M	CO4
Q 7	In the inverter circuit, What is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required relation between $Z_{p.u}$ and $Z_{p.d}$ if the NMOS inverter is to be driven from another NMOS inverter.	10M	CO2
Q 8	Explain the structures of n MOS enhancement mode, depletion mode and p-MOS enhancement mode transistors.	10M	CO1
Q 9	(a) With neat sketches explain different fabrication process of CMOS in detail (or) (b) Design the CMOS implementation of 4 to 1 Mux using transmission gate	10M	CO1 & CO2

SECTION-C 40Marks

Each Question Carries 20 Marks Note: Qno 10 is compulsory attempt any one question from Qno 11 & Qno 12

Q 10	<p>(a) Write a VHDL code for 4*16 decoder using behavioral style of modeling</p> <p>(b) Derive the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region?</p>	[12+8]	CO4 & CO1
Q 11	<p>What is stick diagram and explain about different symbols used for components in Stick diagram .Design a stick diagram and layout for the CMOS logic shown below $Y = (AB+CD)'$</p>	20M	CO3
Q 12	<p>(a) Discuss the lambda based design rules with neat sketches</p> <p>(b) Draw the circuit diagram 4*4 barrel shifter using complementary transmission gate and explain its shifting operation</p>	[10+10]	CO1 & CO2