

## UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

**End Semester Examination, May 2019** 

Course: Digital Systems Semester: 4th

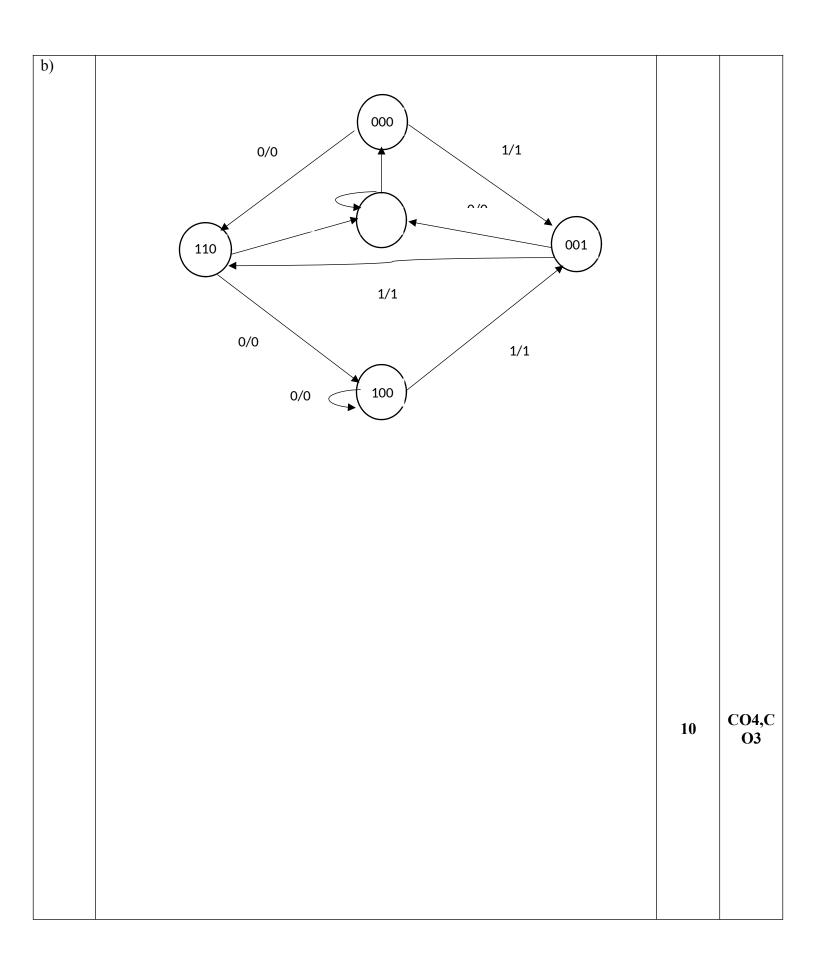
**Program: B.tech Electronics and Communication** 

Time 03 hrs.

Course Code: ECEG-2015 Max. Marks: 100

Instructions: A'should be read as (inverted form of A) and so forth, ∑m---sum of product. All notations and abbreviations are usual notations for digital systems

	ations are usual notations for digital systems SECTION A		
S. No.		Marks	CO
1.	Find the minterms of the function $Y(A,B,C) = AB'+C'$	5	CO2
2.	Minimize the following expressions using K-Map $Y(A,B,C,D)=\sum m(0,2,4,7,8,10,12,13))$	5	CO2
3	Design a combinational logic circuit with four input variables that will produce logic 1 when the number of 1s in the input is even	5	CO3
4	Implement the following Boolean expression using multiplexer Y=(A+B).(A'+B+C).(A+B')	5	CO3
	SECTION B		
5	Develop and analyze a serial in parallel out and parallel in serial out shift register with D-Flip flop	10	CO4
6.	Design a updown 2-bit synchronous counter with D Flipflop	10	CO4
7.	Explain with the help of a circuit diagram the operation of diode transistor logic(DTL) two input NAND gate	10	CO5
8	Implement the following output functions using a suitable PLA $F(A,B,C,D)=\sum m(3,7,8,9,11,15)$	10	CO5
	SECTION-C		
9(a)	Design an asynchronous four bit binary counter. Draw its timing waveform	10	CO4
b)	Design a synchronous binary counter with a counting sequence 0-2-5-6 with J-K Flip flop and repeat. all the undesired states must go back to 000 in the next clock cycle.	10	CO3,C O4
10a)	Design a sequence generator for the sequence 0-2-4-5-1-7-6	10	CO4.C O3



Name:

**Enrolment No:** 



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SECTION A

S. No.								Marks	CO
1	Convert the following Boolean function into standard SOP Y(A,B,C)=AB+AC'+BC						5	CO2	
2	Minimize		following	expressions	using	K-Map	Y(A,B,C,D)=	5	CO2

	$\sum m(0,1,2,3,4,5,6,7,11,13,14)$		
3	Design a combinational logic circuit with three input variables that will produce logic 1 when more than one input variables are logic zero	5	CO3
4	Implement the following Boolean expression using multiplexer Y=A'BC'+AB'C'D+A'B'D+A'CD	5	CO3
	SECTION B		-
5	Develop and analyze a serial in serial out and parallel in parallel out shift register with D Flip-flop	10	CO4
6	Design a up-down two bit synchronous counter with D-Flipflop	10	CO4
7	Explain with the help of a circuit diagram the operation of Transistor transistor logic(TTL) two input NAND gate	10	CO5
8	Implement the following output functions using a suitable PLA $F(A,B,C,D)=\sum m(3,4,5,710,14.15)$	10	CO5
	SECTION-C		
9(a)	Design an asynchronous binary decade counter. Draw its timing waveform	10	CO4
b)	Design a 3-bit synchronous binary counter with a counting sequence 7-6-5-4-1 with T-Flip-flop and repeat . all the undesired states must go back to 7 in the next clock cycle.	10	CO3,C O4
10a)	Design a sequence generator using D-Flipflop to generate the sequence 101100110	10	CO4,C O3
b)		10	CO3,C O4

