Name:

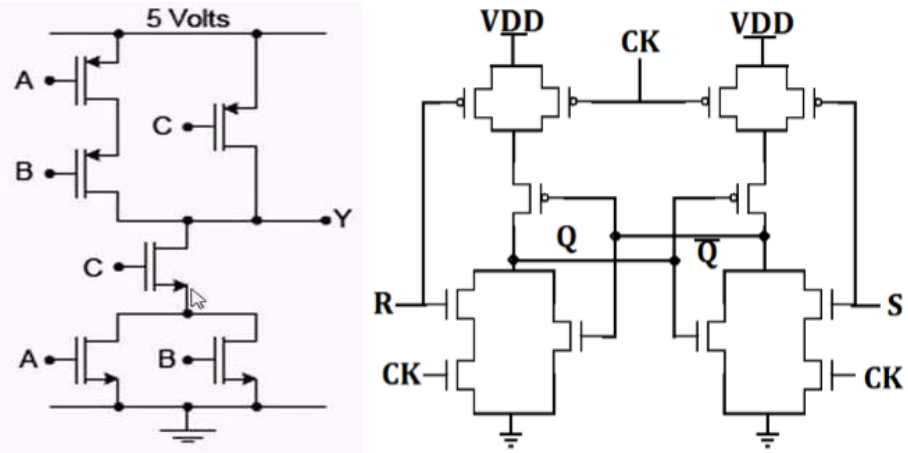
Enrolment No:

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2018

Programme Name: B. Tech (Electronics Engineering) **Semester : VII**
Course Name : VLSI Design **Time : 03 hrs**
Course Code : ELEG-405 **Max. Marks : 100**
Nos. of page(s) : 02
Instructions: Assume any data in programming, if required.

SECTION A (4 x 5 = 20 Marks)

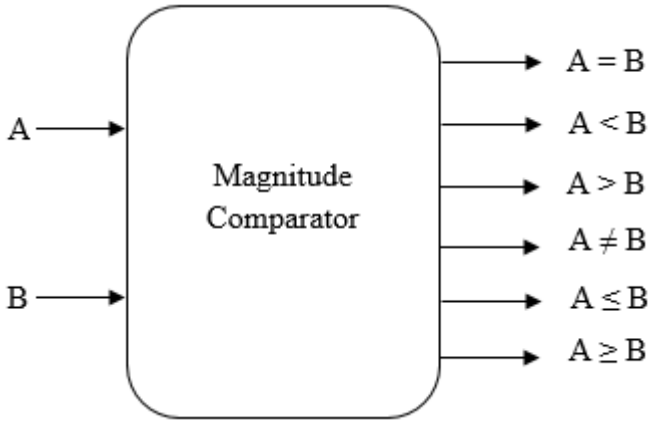
Attempt *all* the questions

S. No.		Marks	CO
Q.1	Why does present VLSI circuits use MOSFETs instead of BJTs?	**5**	**CO1**
Q.2	Realize the output of the logic diagram shown in fig. 1  (a) (b) Fig. 1 CMOS Realization	**5**	**CO4**
Q.3	What are the different styles of modeling followed in VHDL based design. Design (3 x 8) decoder using behavioral VHDL model.	**5**	**CO5**
Q.4	**(a)** If the NMOS device has $\mu_n.C_{ox}$ = 100 µA/V^2, W = 10 µm and L = 1 µm. Find the value of drain current that results the NMOS operation in cutoff, triode and saturation regions. **(b)** Compare NMOS and PMOS based on their performance parameters.	**5**	**CO2**

SECTION B (4 x 10 = 40 Marks)

Attempt *all* the questions

Q.5	Discuss the ASIC Design Flow in detail and detail the different abstraction levels in ICs with example.	**10**	**CO1**
Q.6	What is the significance of stick diagram and layout diagram for understanding MOSFET design? Draw the stick diagram and layout design of 2 input NAND and XOR gate based on CMOS logic.	**10**	**CO3**
Q.7	Detail the functionality of enhancement type NMOS under different regions. Explain the drain voltage characteristics and transfer characteristics in detail	**10**	**CO2**

Q.8	Draw the voltage transfer curve for the CMOS inverter and derive the mathematical expression to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for CMOS inverter circuit and detail the functionality.	**10**	**CO2**
SECTION-C (2 x 20 = 40 Marks) **Attempt *any two* the followings**			
Q.9	**(a)** Draw the cross sectional view of CMOS. Detail all the steps and fabrication process of CMOS using P-Well Process. **(b)** Draw the FPGA design flow used for synthesis the logic. Draw the architecture of any one of the FPGA and explain the functionality: XC 3000, SPARTAN 6, Virtex 5.	**10** **10**	**CO3**
Q.10	**(a)** Compare the all PLD technology and realize the following functions using all technology at gate level and N-MOSFT level. $F_1 = abcd + \bar{a}bcd + \bar{a}bc\bar{d} + ab\bar{c}\bar{d}$ $F_2 = abcd + \bar{a}bcd + a\bar{b}cd + a\bar{b}c\bar{d}$ $F_3 = abcd + \bar{a}b\bar{c}d$ $F_4 = a\bar{b}c\bar{d} + \bar{a}bcd + \bar{a}bc\bar{d} + a\bar{b}cd$ **(b)** Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA.	**10** **10**	**CO4**
Q.11	The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …. An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison. For example, a magnitude comparator of two 1-bits, (A and B) inputs would produce the following three output conditions when compared to each other. This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the case of 64-bit comparator for the different logic functions.  Fig.2 **(a)** Develop the VHDL/ Verilog HDL code to support the functionality of design **(b)** Estimate the different test cases and test benches of the design. **(c)** Design the MOSFET level layout of the design.	**20**	**CO5**

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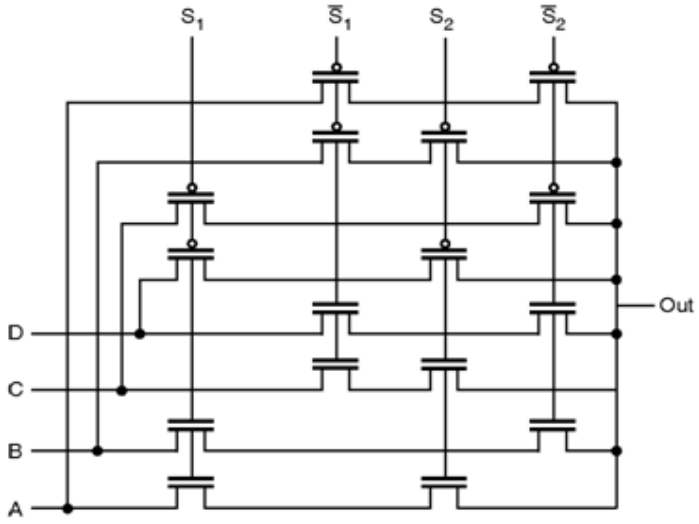
SECTION A (4 x 5 = 20 Marks)

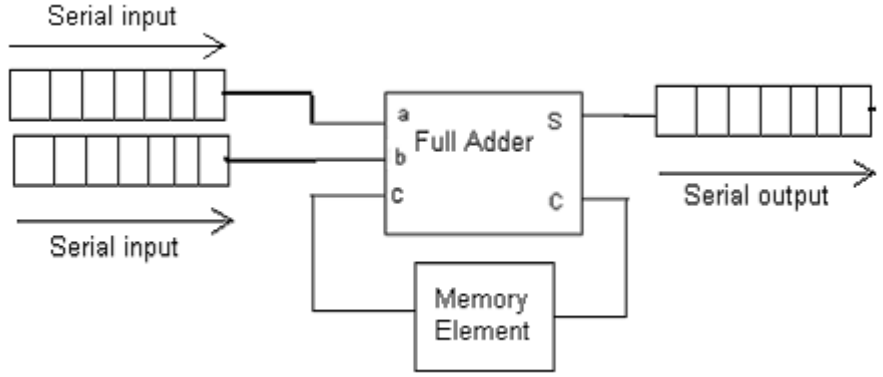
Attempt *all* the questions

S. No.		Marks	CO
Q.1	What is ASIC ? List the different abstraction levele of ICs and suggest the suitable examples.	**5**	**CO1**
Q.2	Realize the output of the logic diagram shown in fig. 1  Fig. 1 CMOS Realization	**5**	**CO4**
Q.3	What are the different styles of modeling followed in VHDL based design. Design (2 x 4) decoder using behavioral VHDL model.	**5**	**CO5**
Q.4	**(a)** If the NMOS device has $\mu_n.C_{ox}$ = 100 µA/V^2, W = 10 µm and L = 1 µm. Find the value of drain current that results the NMOS operation in cutoff, triode and saturation regions. **(b)** Compare NMOS and PMOS based on their performance parameters.	**5**	**CO2**

SECTION B (4 x 10 = 40 Marks)

Attempt *all* the questions

Q.5	Derive the mathematical expressions to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for NMOS inverter circuit and detail the functionality with voltage transfer characteristics with resistive load.	**10**	**CO2**
Q.6	What is the significance of stick diagram and layout diagram for understanding MOSFET design? Draw the stick diagram and layout design of 2 input NOR and XOR gate based on CMOS logic.	**10**	**CO3**

Q.7	Detail the functionality of enhancement type PMOS under different regions. Explain the drain voltage characteristics and transfer characteristics in detail	**10**	**CO2**
Q.8	Explain the role of Noise Margin and speed of operation of low power VLSI digital circuits. A logic gate is defined by the following volatge levels $V_{OH} = 5\,V$ $V_{OL} = 0.2\,V$ $V_{IH} = 2.5\,V$ $V_{IL} = 0.8\,V$ Find the noise margin of this gate.	**10**	**CO3**
SECTION-C (2 x 20 = 40 Marks) **Attempt *any two* the followings**			
Q.9	**(a)** Draw the cross sectional view of CMOS. Detail all the steps and fabrication process of CMOS using P-Well Process. **(b)** Draw the FPGA design flow used for synthesis the logic. Draw the architecture of any one of the FPGA and explain the functionality: XC 4000, SPARTAN 3E, Virtex 7.	**10** **10**	**CO3**
Q.10	**(a)** Compare the all PLD technology and realize the following functions using all technology at gate level and N-MOSFT level. $F_1 = wxyz + \bar{w}xyz + \bar{w}xyz + wx\bar{y}\bar{z}$ $F_2 = wxyz + \bar{w}xyz + w\bar{x}yz + w\bar{x}y\bar{z}$ $F_3 = wxyz + +\bar{w}x\bar{y}z$ $F_4 = w\bar{x}y\bar{z} + \bar{w}xyz + \bar{w}xy\bar{z} + w\bar{x}yz$ **(b)** Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA.	**10** **10**	**CO4**
Q.11	Serial adder is the one which would accept bit by bit input of the n-bit numbers and there is a bit by bit output of the n-bit Sum. In this adder we would be required one full adder and a memory element. Hence It require lesser hardware.  **(a)** Develop the VHDL/ Verilog HDL code to support the functionality of design **(b)** Estimate the different test cases and test benches of the design. (**c)** Design the MOSFET level layout of full adder design.	**20**	**CO5**