Roll No: ----------

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

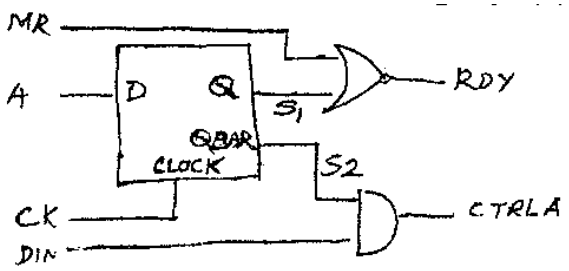
End Semester Examination – April, 2017

Program/course: B. Tech / EE | **Semester – VIII**
Subject: VHDL | **Max. Marks : 100**
Code: ELEG-434 | **Duration : 3 Hrs**
No. of page/s : 2

Section –A

Note: Answer all of the following **5x4=20 Marks**

1. Write the VHDL behavioral description of JK-Flip-flop with active low clock, set and reset using process statement
2. Write the VHDL code for the following circuit in structural model



3. Explain the functionality of Logic Array Block of Flex 10K series PLD.
4. Write the Verilog code for the following Boolean function using if-else statement.

$$f = x_1x_2 + \bar{x}_2x_3$$

5. Write short notes on FPGA and CPLD.

Section –B

Note: Answer all of the following **4x10=40 Marks**

6. List out the salient features and explain the architecture of Altera MAX 5000 programmable logic device.
7. Construct a Bi-polar SRAM cell and explain the working principle with different modes of operation.

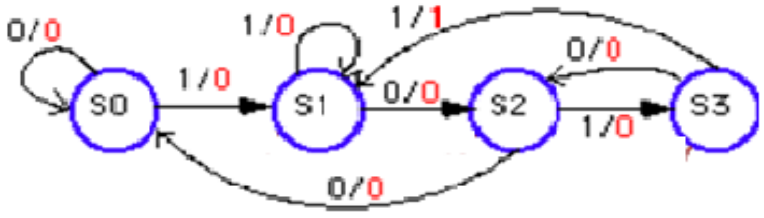
8. Analyze the following design terms in the VLSI design cycle
   a) Architectural Design
   b) Functional Design
   c) Logic Design
   d) Circuit Design
   e) Physical Design
9. a) Write the Verilog code for a 4x1 Multiplexer using case statement.—5 Marks
   b) Derive the circuit for the piece of code given below and comment on the same—5 Marks

```
module electronics(x,clock,Q1,Q2)
    input x, clock;
    output reg Q1, Q2;
    always@(posedge clock)
    begin
    Q1=x;
    Q2= Q1;
    end
    end module
```

Section –C

Note: Answer all of the following **2x20=40 Marks**

10. a) Design the synchronous sequential circuit for the following state graph. Choose flip-flop of your choice—[10] Marks
    b) Write the VHDL code for the design using structural model—5 Marks
    c) Write the Verilog code for the design using dataflow model—5 Marks



11. a) Analyze the detailed functional description of Xilinx 4000 series FPGA with neat sketch—15 Marks
    b) Comment on the resource utilization of the FPGA when using VHDL and Verilog styles of modelling—5 Marks.

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Section –A

Note: Answer all of the following **5x4=20 Marks**

1. Compare different keywords of VHDL and Verilog Languages.
2. Design an 8X4 diode ROM using 74X138(Decoder) for the following data starting from the first location 6, 9, 0, C, D, 1, F, D.
3. Write the VHDL code for a T-flipflop with active high clock.
4. Write the Verilog code for the following Boolean function using if-else statement.

$$f = x_1 x_2 + \overline{x}_2 x_3$$

5. How process statements can be used to control when a process is activated in VHDL

Section –B

Note: Answer all of the following **4x10=40 Marks**

6. Visualize the VLSI design methodology of the three domains in Gajski's Y-chart.
7. Implement the given 3-input, 4- output truth table of a combinational circuit using PAL. Write the VHDL and Verilog code using Data Flow model.

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

8. List out the salient features and explain the architecture of Flex 10K series programmable logic device.
9. a) Write the Verilog code for a 3x8 Decoder using case statement.—5 Marks

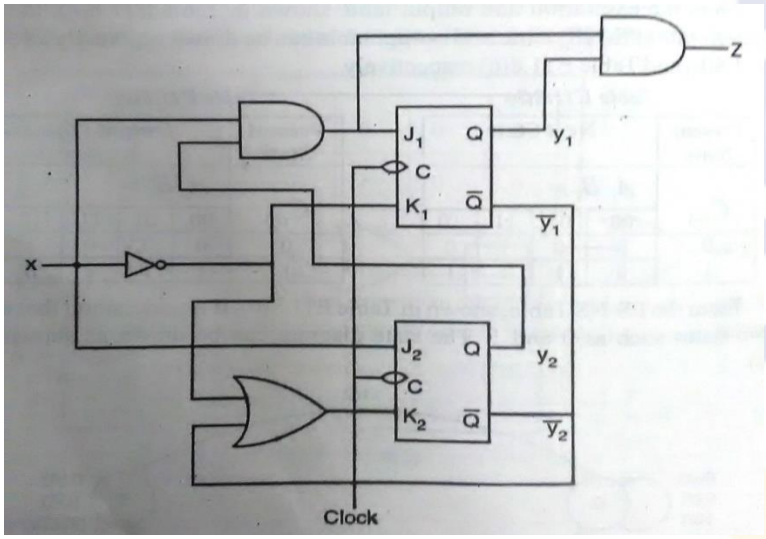
   b) Derive the circuit for the piece of code given below and comment on the same—5 Marks

```
module electronics(x,clock,Q1,Q2)
    input x, clock;
    output reg Q1, Q2;
    always@(posedge clock)
    begin
    Q1=x;
    Q2= Q1;
    end
    end module
```

Section –C

Note: Answer all of the following **2x20=40 Marks**

10. Analyze the given sequential circuit, write the VHDL and Verilog codes using structural model.



11. a) Construct a Bi-polar SRAM cell and explain the Holding, Reading and writing state modes of operation.—10 Marks

    b) Analyze the detailed functional description of Xilinx 4000 series FPGA with neat sketch.—10 Marks

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