# ABSTRACT

Orthogonal Frequency Division Multiple Access (OFDMA) is a promising multi-user version of a popular Orthogonal Frequency Division Multiplexing (OFDM) scheme. OFDMA is used for high data rate applications with the IEEE.802.16e standard and multiple access is achieved in OFDMA by assigning subsets of subcarriers to individual users which are transmitted at different frequencies. It has high spectral efficiency and fading immunity when the signal is travelling is in a non-ideal channel. Conventional OFDMA uses efficient IFFT and FFT algorithms along with the equalizer algorithms in the receiver to mitigate the inter symbol interference caused by the multi path propagation. FFT Window positioned OFDMA shifts the position of the FFT window by the amount of delay caused by the symbols during travelling to the receiver via multiple paths. It starts the FFT processing on the received symbols only after ensuring that all the symbols have been arrived at the receiver thus mitigating the signal interference. Both the conventional OFDMA and the window positioned OFDMA have been implemented in this dissertation. Vertex-5 Xilinx FPGA board has been used for the synthesizing the results on the hardware. Modelsim10.2 & MATLAB are used to carry out the simulation results. SNR vs BER performance was evaluated for all the results. 2D-FFT algorithm was used over regular FFT algorithm to improve the system level of parallelism and efficient use of bandwidth. Power-delay profiles of International Telecommunication Union (ITU) have been studied and the delays provided by the ITU are considered as three test cases for introducing the appropriate delay for the FFT window. Variable length FFT processor has been implemented for the OFDMA which can actually shift the size of the input to 128-pt FFT, 512-pt FFT, 1024-pt FFT and 2048-pt FFT depending on the channel and bandwidth.