

CHAPTER-5
HARDWARE MODELLING &
CHIP DESIGN

The chapter focuses on the chip design and implementation of hardware system on FPGA for both section (Helmet node and two-wheeler node) as discussed in chapter-3. The high speed controller is designed with the help of VHDL programming language in Xilinx 14.2 ISE software and synthesized on Virtex-5 FPGA, which is an optimal solution for the intelligent helmet. The function simulation is also carried to test the different test cases with Modelsim 10.1b. Performance analysis is done for the both designed controllers.

The controller is designed with the help of VHDL programming language in Xilinx 14.2 ISE software and then synthesized on Virtex-5 FPGA. The Modelsim 10.1b simulation is done to test the different test cases.

5.1 Helmet Node

The controller is designed for four analog inputs from flex sensor. As flex sensors gives analog output and controller only understands the digital values so to process the signal analog to digital converter is also placed with the sensor inputs to the controller. The average value of all the four sensors are taken. This value is then displayed on LCD to verify the data when actual hardware implementation is done. The same value is transmitted to two wheeler node wirelessly through RF modem.

The RTL view transmitter section of the intelligent helmet system is shown in Fig.5.1. It shows all the possible inputs and outputs of the designed controller. Table 5.1 discussed the details of the pins .

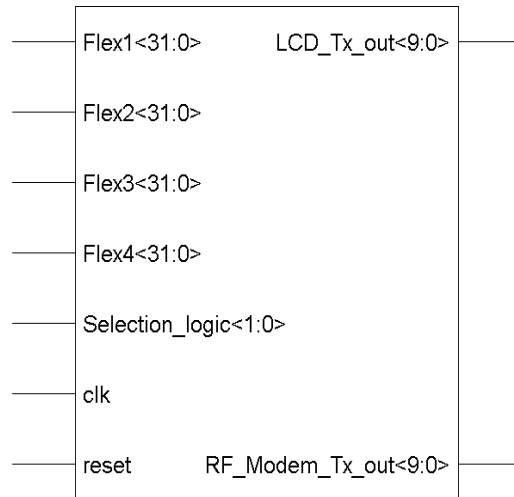


Fig. 5.1 RTL view of helmet node controller

Table 5.1 Pin description of controller of helmet node

Pin	Function
Flex1<31:0>	It is the input of the flex sensor 1
Flex2<31:0>	It is the input of the flex sensor 2
Flex3<31:0>	It is the input of the flex sensor 3
Flex4<31:0>	It is the input of the flex sensor 4
Selection_logic<1:0>	Input selection logic to get the input data with respect to flex1, flex 2, flex 3, flex 4
Clk	The clock signal at the 'helmet node'
Reset	The reset signal to synchronize the clock input signal
LCD_out<9:0>	The values of flex1, flex 2, flex 3 and flex 4 is displayed on LCD
RF_Modem_Tx_out<9:0>	The Transmitted data displayed on LCD

5.1.1 Simulation and Synthesis Results for Helmet Node Controller

The controller is designed with the help of VHDL programming language in Xilinx 14.2 ISE software and then synthesized on Virtex-5 FPGA. The Modelsim 10.1b simulation is done to test the different test cases.

The internal architecture is shown in Fig.5.2. It has four inputs and one output. The four input options are to interface sensor. In the proposed system only three sensor inputs are used and fourth input is kept zero. In case the system needs to calculate the impact on head after accident then fourth sensor is to be connected. Sensors are analog in nature so ADC is placed between each input and controller. The output is taken serially and transmitted to RF modem through buffer and same is also displayed on LCD.

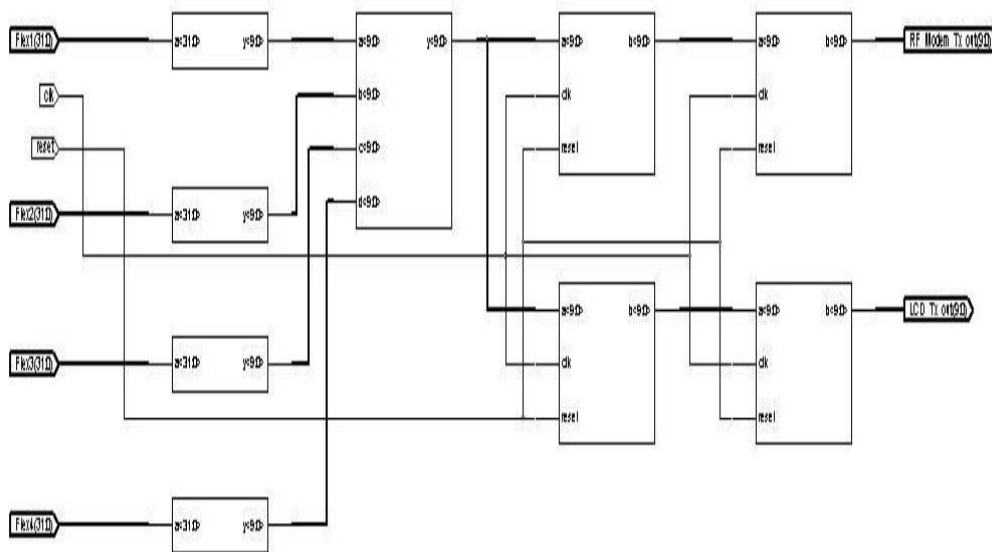


Fig.5.2 Internal architecture of the controller for helmet node

The modelsim wave output of the helmet node is shown in Fig.5.3 and Fig.5.4. The Fig.5.5 presents the output for 1 test case. The Fig.5.6 presents the output for 5 test cases. In the waveform flex1, flex 2, flex 3 and flex4 presents the flex sensor inputs. The clk and reset are the default inputs. The selection of sensor values is done based on slection_logic[1:0]. The output of flex 1, flex 2, flex 3 and flex 4 first converted to digital using 10 bits ADC shown in Fig.26 ADC1[9 :

0], ADC2 [9 : 0], ADC3 [9 : 0] and ADC4 [9 : 0] corresponding to flex1, flex2, flex 3 and flex4, USART_ in shows the value of USART transmission. In the same way lcd_tx_in [9:0] and lcd_tx_out [9:0] shows LCD input and output. Rf_modem_tx_in [9:0] and Rf_modem_tx_out [9:0] present the input and output of the RF modem input and output.

The simulation waveforms are tested for following values.

Case 1: flex1 = 215 , flex 2 =216 , flex 3 = 209 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 214.

Fig.5.3 shows the simulation waveform for test case -1.

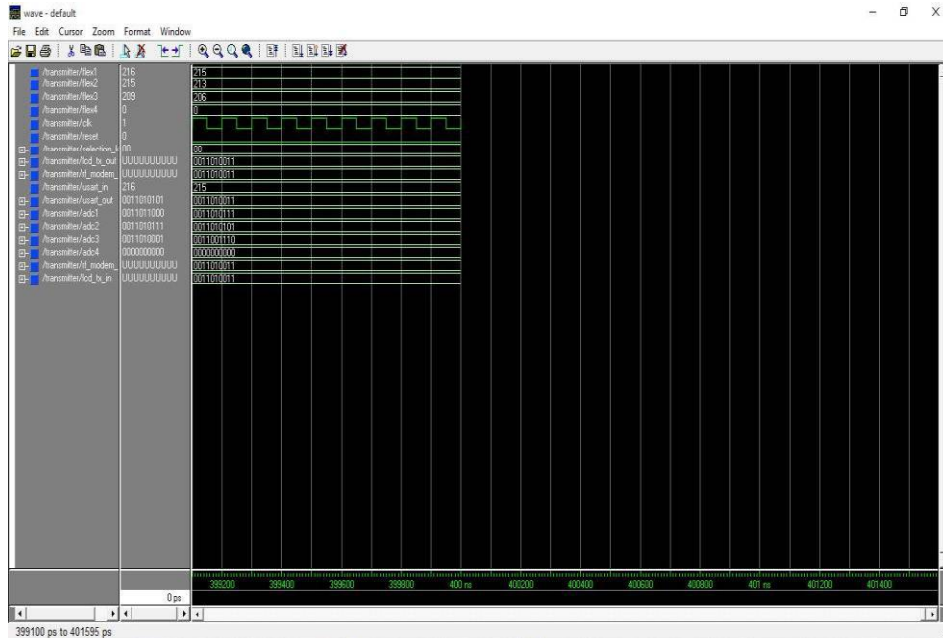


Fig.5.3 Simulation waveform for test case -1

Case 2: flex1 = 216 , flex 2 =215 , flex 3 = 205 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 212.

Case 3: flex1 = 215 , flex 2 =213 , flex 3 = 206 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 212.

Case 4: flex1 = 215 , flex 2 =216 , flex 3 = 211 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 214.

Fig.5.4 shows the simulation waveforms for test case 1 to 4.

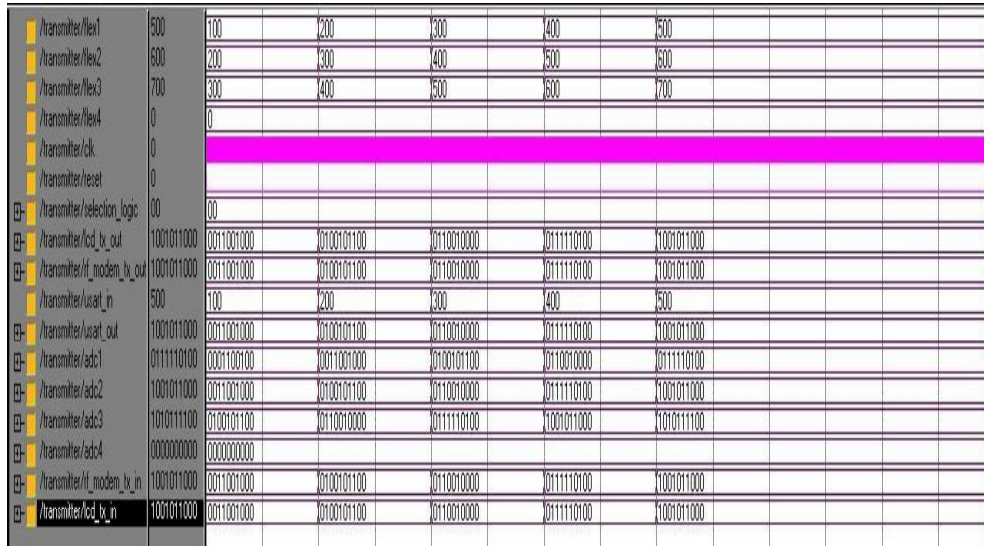


Fig.5.4 Simulation waveform for test case 1 to 4

Case 5: flex1 = 100 , flex 2 =200 , flex 3 = 300 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0011001000 in binary and 200 in decimal.

Fig.5.5 shows the simulation waveform for test case-5.

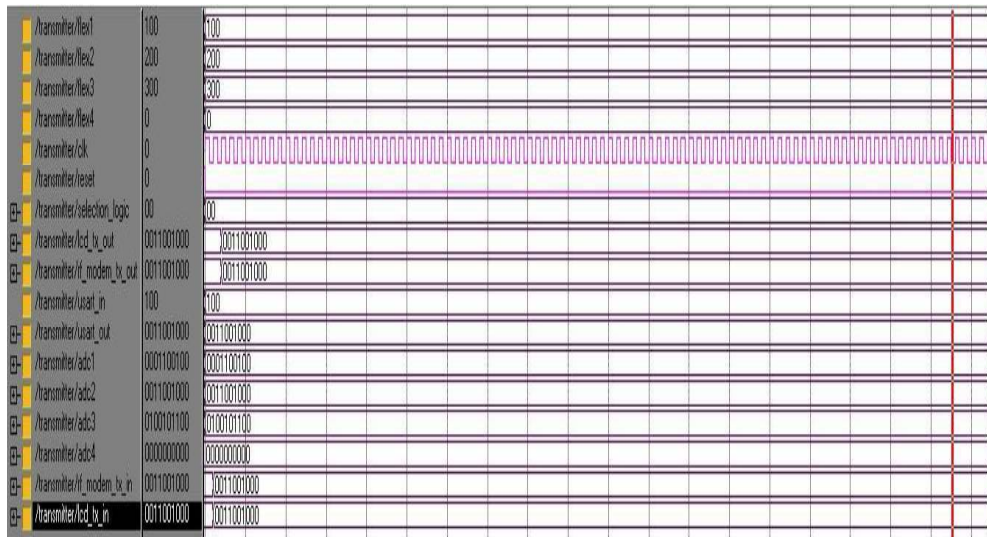


Fig. 5.5 Simulation waveform for test case-5

Case 6: flex1 = 200 , flex 2 =300 , flex 3 = 400 and flex 4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0100101100 in binary and 300 in decimal.

Case 7: flex1 = 300 , flex 2 =400 , flex 3 = 500 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0110010000 in binary and 400 in decimal.

Case 8: flex1 = 400 , flex 2 =500 , flex 3 = 600 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 0111110100 in binary and 500 in decimal.

Case 9: flex1 = 500 , flex 2 =600 , flex 3 = 700 and flex4 = 0 and corresponding output is Rf_modem_tx_out [9:0] = 1001011000 in binary and 600 in decimal.

Fig.5.6 shows the simulation waveform for test case 5 to 9.

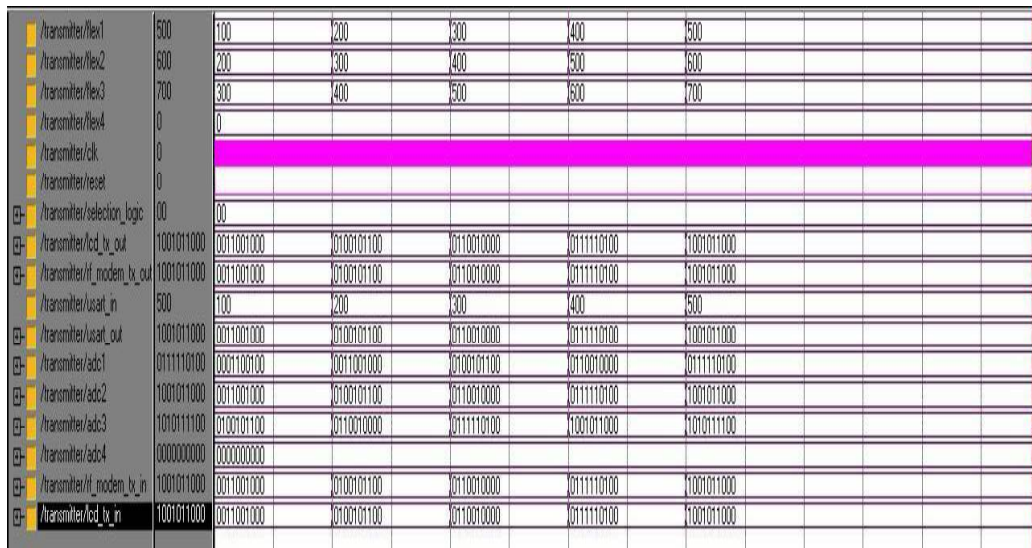


Fig.5.6 Simulation waveform for test case-5 to 9

5.1.2 FPGA Synthesis Report of Helmet Node

The synthesis of designed system is done on Spartan-6 FPGA with the target device Xc6slx-45-2csg324. The hardware summary report displays the utilization of LUTs, inputs and output, flip flops, value of slice registers and buffers and CPU memory etc. Table-5.2 describes the hardware summary report of helmet node. The timing summary shows the value of ‘minimum’ and ‘maximum’ clock timing and ‘frequency’ support.

Timing Summary

Speed Grade = ‘2’

‘Minimum’ Period value = ‘1.280ns’

‘Maximum’ Frequency value = ‘781.250MHz’

‘Minimum’ Arrival time value before clock = ‘24.084ns’

‘Maximum’ Output time required after clock = ‘4.162ns’

CPU memory usage = ‘251564 kilobyte’

Table 5.2 describes the hardware summary report of helmet node.

Table 5.2 Hardware Summary report of helmet node

Transmitter Project Status			
Project File:	ADC.xise	Parser Errors:	No Errors
Module Name:	Transmitter	Implementation State:	Synthesized
Target Device:	xc6slx45-2csg324	• Errors:	No Errors
Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	20	54576	0%
Number of Slice LUTs	779	27288	2%
Number of fully used LUT-FF pairs	0	799	0%
Number of bonded IOBs	118	218	54%
Number of BUFG/BUFGCTRLs	1	16	6%

5.2 Two-wheeler Node

The two wheeler controller is designed with Xilinx 14.2 ISE using the VHDL programming language. The synthesis of designed system is done on Virtex-5 FPGA. The simulation is done on Modelsim 10.1b to test the different cases results analysis.

Fig.5.7 shows the RTL view of two wheeler section. It shows all the possible inputs and outputs of the designed controller. The detail of the pins is discussed in Table 5.3.

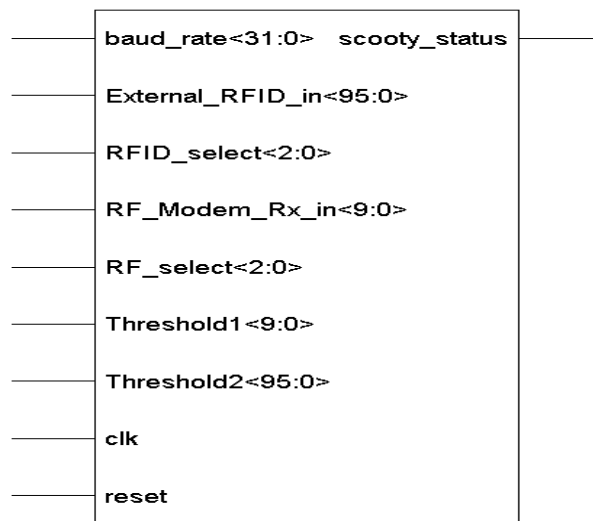


Fig. 5.7 RTL view of receiver node controller

Table 5.3 Pin description of two-wheeler controller

Pin	Function
Baud_rate <31:0>	It is the input signal to the two wheeler which is used to assign the baud rate.
External_ RFID_in <95:0>	Input signal for receiver to RFID as 12 byte data
RFID_ Select<2:0>	To select the comparison operation, select the logic for the RFID comparator.
RF_Modem_Rx	Modem to received data

_in<9:0>	
RF_select<2:0>	To select the comparison operation, select logic for the RF comparator.
Threshold1<9:0>	Input signal to the two wheeler as threshold
Threshold2 <95:0>	Input signal to the RFID module as 12 byte
Clk	Clock signal
Reset	The reset signal to synchronize to clock signal
Scooty_status	Output to make the two wheeler in ‘On’ and ‘Off’ state

5.2.1 Simulation and Synthesis Results for Two-wheeler Controller

The two wheeler node is designed to receive the average value of sensors which is transmitted by helmet node. It also extracts the code from RFID tag. These two signals are then given as input to the comparator and matched with pre-defined values of sensor and RFID tag. If both the signals are matched with pre-defined values then only output is given as logic ‘1’ otherwise logic ‘0’ is generated by controller. The internal architecture of two wheeler node is shown in Fig. 5.8.

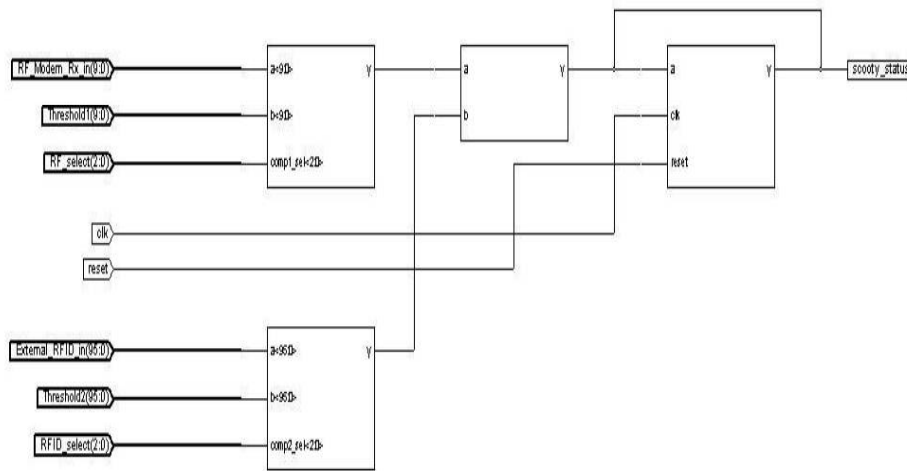


Fig.5.8 Internal architecture of the controller of two wheeler node

The modelsim simulation of the two-wheeler is done to make it 'ON' and 'OFF' which is displayed in Fig-5.9, 5.10, 5.11. The 'scooty/receiver' is written as synonym for 'two-wheeler'.

Fig.-5.9 & 5.10 shows the modelsim simulation results when the status of scooty is 'ON' and Fig.5.11 shows the result for two wheeler when the status of scooty is 'OFF'. Relay is taken as intermediate device between the status of scooty and cumulative data. The baud rate is chosen same as of RF modem which is '9600' bps. USART_RF is designed to receive data and gives the comparative output of the RF modem, RF_Modem_ Rx_in <9:0> and threshold1. RFID comparator gives output to USART_RFID and to the External_RFID_in[95:0] and threshold2 [95:0]. The status of Relay as 'ON' or 'OFF' is decided on the basis of AND operation on RF data and USART data and the status of scooty as 'ON' or 'OFF' is changed.

The simulation waveforms are tested for following values-

Case 1: The Baud_rate <31:0> is '9600'; the value of External_ RFID_in <95:0> is '1'd4000 (decimal)', data received by RF_Modem_ Rx_in<9:0> is '214', sensor average value Threshold1 is '212', RFID data threshold 2 is '1'd 2000' (decimal), then after applying AND operation on USART_RF as '1', USART_RFID as '1', which makes the relay_on_off as '1' and Two wheeler_status _status as '1'. Two wheeler_status is 'ON'.

Case 2: The Baud_rate<31:0> is '9600', the value of External_ RFID_in <95:0> is '1'd5000' (decimal), data received by RF_Modem_Rx_in<9:0> is '213', sensor average value Threshold1 is '212', RFID data threshold 2 is '1'd 2000' (decimal) then after applying AND operation on USART_RF as '1', USART_RFID as '1', which makes relay_on_off as '1' and Two wheeler_status _status = '1'. Two wheeler_status is 'ON'.

Case 3: The Baud_rate<31:0> is '9600', the value of External_ RFID_in <95:0> is '1'd6000'(decimal), RF_Modem_ Rx_in<9:0> is '214', sensor average value Threshold1 is '212', RFID data threshold 2 is '1'd 2000' (decimal) then

after applying AND operation on USART_RF as '1', USART_RFID as '1', Relay_on_off as '1' and Two wheeler_s tatus _status = '1'. Two wheeler_ status is 'ON'.

Case 4: The Baud_rate<31:0> is '9600', the value of External_RFID_in <95:0> is '1'd7000'(decimal), RF_Modem_Rx_in<9:0> is '213', sensor average value Threshold1 is '212', RFID data threshold 2 is '1'd 2000' (decimal) then after applying AND operation on USART_RF as '1', USART_RFID as '1', Relay_on_off as '1' and Two wheeler_status _status = '1'. Two wheeler_status is 'ON'.

Case 5: The Baud_rate <31:0> is '9600', the value of External_RFID_in <95:0> is '1'd4000' (decimal), RF_Modem_Rx_in<9:0> is '200', sensor average value Threshold1 is '212', RFID data threshold 2 is '1'd 2000' (decimal) then output USART_RF as '0', Relay_on_off as '0' and Two wheeler_status _status = '0'. Two wheeler_status is 'OFF'.

Fig.5.9 & Fig.5.10 shows the modelsim simulation for scooty in 'ON' condition.

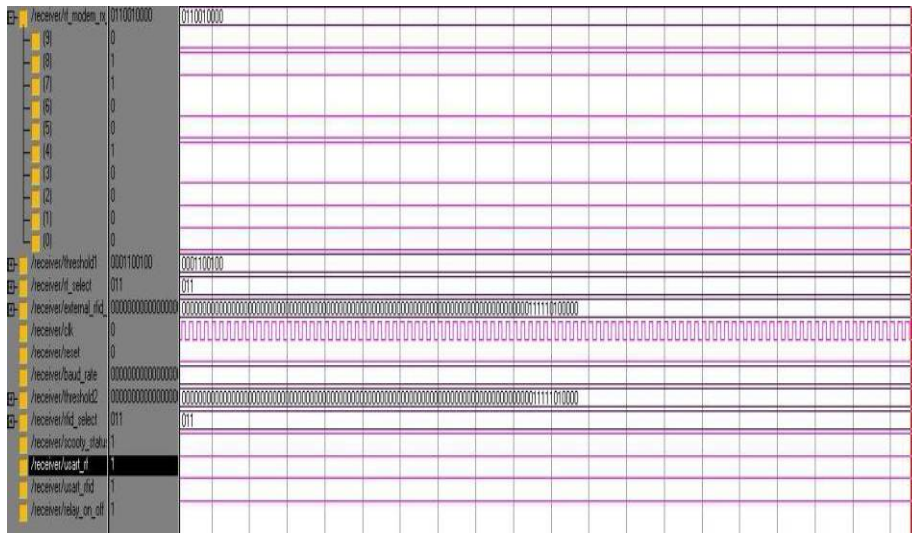


Fig.5.9 The results of modelsim simulation of receiver (scooty on)

‘minimum’ and ‘maximum’ clock timing and frequency support. Table 5.4 describes the hardware summary report of the two-wheeler node.

Table 5.4: Hardware summary report of two-wheeler node

Receiver Project Status				
Project File:	ADC.xise	Parser Errors:	No Errors	
Module Name:	Receiver	Implementation State:	Synthesized	
Target Device:	xc6slx45-2csg324	• Errors:	No Errors	
Device Utilization Summary (estimated values)				[1]
Logic Utilization	Used	Available	Utilization	
Number of Slice Registers	2	54576	0%	
Number of Slice LUTs	249	27288	0%	
Number of fully used LUT-FF pairs	2	249	0%	
Number of bonded IOBs	218	218	100%	

Timing Summary:

Speed Grade = ‘2’

‘Minimum’ Period value = ‘0.980 ns’

‘Maximum’ Frequency Value = ‘781.250 MHz’

‘Minimum’ Arrival time value before clock = ‘6.312’ ns

‘Maximum’ output time required after clock = ‘5.214’ ns

CPU memory usage= ‘249452 kilobytes’

5.3 Result Analysis from Simulation and Synthesis of Designed Controller

Helmet Node

The controller for the helmet node is designed with hardware description language environment and results are analyzed with Virtex-5. The controller is designed with four analog inputs from flex sensor and two serial outputs for LCD and RF modem. The LCD is connected to display the cumulative data from flex sensors. The working frequency of the designed controller is 781.250 MHz which is very high as compared to existing controllers like AVR Atmega-16 which works on max. frequency of 16 MHz. The minimum period value is calculated as

'1.280ns', arrival time is '24.084ns' and the CPU memory usage is '251564 kilobytes'. The designed chip can be a boon to VLSI industries as an optimal solution to the system.

Two- Wheeler Node

The hardware description language environment is used to design two wheeler controller and results are analyzed with Virtex-5. The operating frequency of the designed two wheeler controller is '781.250 MHz' which is higher as compared to existing controllers in market like AVR Atmega-16 which operates on max. frequency of 16 MHz. The arrival time before clock as 'minimum' and after clock as 'maximum' are observed as '6.312 ns' and '5.214 ns' respectively. The minimum period value is calculated as '0.980ns' and the total CPU memory usage is '249452 kilobytes'. The designed chip is an optimal solution to the two wheeler section.

5.4 Chapter Summary

Chapter concludes the results analysis of the chip development for the two sections- helmet node and two-wheeler node. A high speed transmitter controller with frequency of 781.250 MHz with is designed for the helmet node. A high speed receiver controller with frequency of 781.250 MHz is designed for the two-wheeler node.